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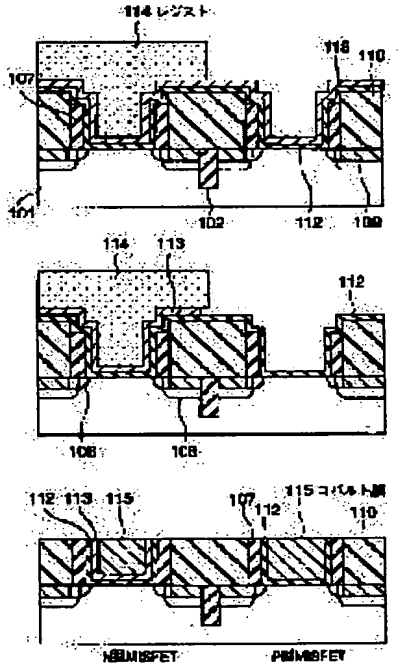
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To enable micronizing a semiconductor device in the case that a gate electrode is formed by using damascene gate technique or the like.
SOLUTION: A process forming a gate electrode is constituted of a process forming a first metal containing film 113 in recessed parts of an N-type and a P-type MIS transistor regions, a process eliminating the first metal containing film formed in the P-type MIS transistor region, and a process forming a second metal containing film 115 on the first metal containing film left in the N-type MIS transistor region and on a gate insulating film 112 in the P-type MIS transistor region. A work function of the metal containing film in contact with a gate insulating film of the N-type MIS transistor is smaller than that of the metal containing film in contact with the gate insulating film of the P-type MIS transistor.



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CLAIMS

[Claim(s)]
[Claim 1] It is the semiconductor device with which the gate electrode of an N type MIS transistor and each P type MIS transistor is formed through gate dielectric film in the crevice formed in the semi-conductor substrate. One [at least] gate electrode of an N type MIS transistor and a P type MIS transistor is constituted by the laminated structure of two or more metal content film. That and it is smaller than the work function of the part of the metal content film with which the work function of the part of the metal content film which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The semiconductor device by which it is characterized.
[Claim 2] It is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which removes the 1st metal content film formed in one field of the 1st or 2nd gate formation field, It consists of a process which embeds the crevice of the field of the both sides of the 1st and 2nd gate formation fields by forming the 2nd metal content film on the 1st metal content film saved to the field of another side of the 1st or 2nd gate formation field, and the gate dielectric film of one field of the 1st or 2nd gate formation field. The inside of said 1st and 2nd metal content film, That it is smaller than the work function of the part of the metal content film of the direction where the work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The manufacture approach of the semiconductor device by which it is characterized.
[Claim 3] It is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which removes the 1st metal content film formed in one field of the 1st or 2nd gate formation field, The process which forms the 3rd metal content film on the 1st metal content film saved to the field of another side of the 1st or 2nd gate formation field, and the gate dielectric film of one field of the 1st or 2nd gate formation field, The process which removes the 3rd metal content film formed in the field of another side of the 1st or 2nd gate formation field, By forming the 2nd metal content film on the 1st metal content film exposed to the field of another side of the 3rd metal content film top saved to one field of the 1st or 2nd gate formation field, and the 1st or 2nd gate formation field It consists of a process which embeds the crevice of the field of the both sides of the 1st and 2nd gate formation fields. The inside of said 1st and 2nd metal content film, That it is smaller than the work function of the part of the metal content film of the direction where the work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The manufacture approach of the semiconductor device by which it is characterized.
[Claim 4] It is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-

conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, It consists of a process which changes the 1st metal content film into the 2nd metal content film by making the matter contained in the 1st metal content film formed in one field of the 1st or 2nd gate formation field, and matter other than this matter react. The inside of said 1st and 2nd metal content film, That it is smaller than the work function of the part of the metal content film of the direction where the work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The manufacture approach of the semiconductor device by which it is characterized.

[Claim 5] It is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which changes the 1st metal content film into the 2nd metal content film by making the matter contained in the 1st metal content film formed in one field of the 1st or 2nd gate formation field, and matter other than this matter react, It consists of a process which changes the 1st metal content film into the 3rd metal content film by making the matter contained in the 1st metal content film formed in the field of another side of the 1st or 2nd gate formation field, and matter other than this matter react. The inside of said 2nd and 3rd metal content film, That it is smaller than the work function of the part of the metal content film of the direction where the work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The manufacture approach of the semiconductor device by which it is characterized.

[Claim 6] It is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, It consists of a process which forms the 2nd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface. the inside of the 1st metal content film formed in one field of the 1st or 2nd gate formation field -- this -- among said 1st and 2nd metal content film That it is smaller than the work function of the part of the metal content film of the direction where the work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The manufacture approach of the semiconductor device by which it is characterized.

[Claim 7] It is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, the inside of the 1st metal content film formed in one field of the 1st or 2nd gate formation field -- this -- with the process which forms the 2nd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface It consists of a process which forms the 3rd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface. the inside of the 1st metal content film formed in the field of another side of the 1st or 2nd gate formation field -- this -- among said 2nd and 3rd metal content film That it is smaller than the work function of the part of the metal content film of the direction where the work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least The manufacture approach of the semiconductor device by which it is characterized.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to amelioration of the gate electrode of a semiconductor device and its manufacture approach especially an N type MIS transistor, and a P type MIS transistor.
[0002]
[Description of the Prior Art] For high-performance-izing of an MIS transistor, detailed-izing of a component is indispensable. However, since the silicon oxide used as gate dielectric film now has the low dielectric constant, it has the problem that capacity of gate dielectric film cannot be enlarged. Moreover, since the polish recon used as a gate electrode has high resistivity, it has the problem that low resistance-ization cannot be attained. The proposal of using a metallic material for a gate electrode is made by gate dielectric film to each problem using high dielectric materials.
[0003] However, these ingredients have the fault that it is inferior to thermal resistance compared with the ingredient used now. Then, after performing an elevated-temperature process, the DAMASHIN gate technique is proposed as a technique which can form gate dielectric film and a gate electrode.
[0004] A DAMASHIN gate technique embeds an electrode material to the field which removed the dummy gate after forming in the gate formation schedule field the gate which serves as a dummy beforehand and forming a source drain diffusion layer, and removed the dummy gate, and produces a gate electrode.
[0005] Since the work function of the gate electrode of both transistors cannot be changed if the same metal is used for the gate electrode of N type and a P type MIS transistor when producing a gate electrode using a pellet scene gate technique, the threshold of N type and each P type MIS transistor cannot be rationalized.
[0006] Therefore, the manufacture process using a different gate electrode material is needed with an N type MIS transistor and a P type MIS transistor. Hereafter, an example of such a manufacture process is explained with reference to drawing 20 (a) - drawing 23 (i).
[0007] First, the isolation 502 of STI structure is formed on a silicon substrate 501. Then, silicon oxide 503 of about 6nm of thickness is formed as a dummy insulator layer removed in the future. Furthermore, the laminated structure of the polish recon film 504 of about 150nm of thickness and the silicon nitride 505 of about 50nm of thickness is formed as the dummy gate removed in the future. These dummy insulator layers and the dummy gate are formed using the usual techniques (membrane formation techniques, such as oxidation and CVD, a lithography technique, RIE technique, etc.). Then, the impurity diffused layer for extensions used as the source drain diffusion layer 506 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 504 and silicon nitride 505) as a mask. Then, a gate side-attachment-wall insulator layer with a width of face of about 40nm which consists of a silicon nitride 507 is formed with a CVD technique and a RIE technique (drawing 20 (a)).
[0008] Next, the high concentration impurity diffused layer used as the source drain diffusion layer 508 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 504 and silicon nitride 505) and a gate side-attachment-wall insulator layer (silicon nitriding 507) as a mask. Furthermore, the silicide film (silicide such as cobalt or titanium) 509 with a thickness of about 40nm is formed only in a source drain field by using the dummy gate as a mask with a salicide process technique (drawing 20 (b)).
[0009] Next, silicon oxide is deposited with a CVD method as an interlayer insulation film 510. Furthermore, the front face of the silicon nitrides 505 and 507 is exposed by carrying out flattening of this interlayer insulation film 510 with a CMP technique (drawing 20 (c)).
[0010] Next, the silicon nitride 505 of the dummy gate upper part is alternatively removed to an interlayer

insulation film 510, for example using phosphoric acid. At this time, the silicon nitride 507 is also etched to height extent of the polish recon film 504. Then, the etching technique using the radical of halogen atoms, such as a fluorine, removes the polish recon film 504 alternatively to an interlayer insulation film 510 and the silicon nitride 507, for example (drawing 21 (d)).

[0011] Next, a slot (crevice) is formed by removing dummy silicon oxide 503 by wet etching, such as fluoric acid. Then, Ta 2O5 which is a high dielectric insulator layer as gate dielectric film The film 512 is formed with a CVD method etc. Then, the aluminum film 513 is deposited as a gate electrode (drawing 21 R> 1 (e)).

[0012] Next, a CMP technique is used and it is Ta 2O5. Flattening of the film 512 and the aluminum film 513 is performed until an interlayer insulation film 510 is exposed (drawing 21 (f)).

[0013] Although the process of the above drawing 20 (a) - drawing 21 (f) was performed to the both sides of an N type MIS transistor formation field and a P type MIS transistor formation field, it showed only one field on the drawing. From future processes, the both sides of an N type MIS transistor (N type MISFET) formation field and a P type MIS transistor (P type MISFET) formation field are shown on a drawing.

[0014] It covers except a P type MIS transistor formation field by the resist 514 after the process of drawing 21 (f) using a lithography technique (drawing 22 (g)).

[0015] Next, only a P type field removes the aluminum film 513 by performing wet etching by phosphoric acid. Although the silicon nitride 507 is exposed at this time, in the phosphoric acid of a room temperature, it is hardly etched (drawing 22 R> 2 (h)).

[0016] Next, after removing a resist 514, the cobalt film 515 is deposited on the whole surface as a metal with which a work function is set to about 5eV (drawing 23 (i)).

[0017] Next, using a CMP technique, flattening of the cobalt film 515 is performed until an interlayer insulation film 510 is exposed (drawing 23 (j)).

[0018] According to the above process, as gate electrode structure, N type consists of aluminum film 513, and C-MIS transistor which consists of cobalt film 515 completes P type. Since a work function is about 5eV, it is with an N type MIS transistor and a P type MIS transistor, and, as for about 4.2eV and the cobalt film 515, can optimize the work function of a gate electrode by each, and as for the aluminum film 513, a work function can optimize the threshold electrical potential difference of both transistors.

[0019] However, with the conventional technique mentioned above, a big problem arises to detailed-izing. Hereafter, this problem is explained.

[0020] Drawing 24 (a), drawing 24 (b), and drawing 24 (c) are the top views having shown typically the principal part in drawing 22 (g), drawing 22 (h), and drawing 2323 (j), respectively. The distance between each source drain of an N type MIS transistor and a P type MIS transistor, i.e., the distance between components, is set to D.

[0021] In the process of drawing 22 (h), if a resist 514 is used as a mask and wet etching of the aluminum film 513 of a P type field is carried out, wet etching will advance isotropic. Therefore, etching will go deeply to the field by which the mask was carried out by the resist 514, and as shown in drawing 24 (b), the aluminum film 513 will be etched to an N type field.

[0022] Therefore, the completed transistor structure comes to be shown in drawing 24 (c). That is, a gate electrode will be constituted from an N type field by the aluminum film and cobalt film with which work functions differ mutually. The field where thresholds differ will exist and it becomes impossible therefore, to desire a setup of a low threshold electrical potential difference in an N type MIS transistor.

[0023] The problem mentioned above is examined further. The amount E of etching of the longitudinal direction by wet etching becomes more than height H (refer to drawing 22 (h)) of the aluminum film usually etched. In the example mentioned above, since height H of the aluminum film is about 150nm, the lateral amount E of etching is set to 150nm or more. Therefore, in order to avoid the problem mentioned above, it is necessary to make distance D between components into twice [more than / more than], i.e., 300nm, the lateral amount E of etching, and it becomes very difficult to perform detailed-ization. Although detailed-ization of extent which is making height H of the aluminum film low is attained, since gate resistance increases by reduction of height H of the aluminum film, it does not become an essential solution.

[0024] Moreover, with the conventional technique mentioned above, a big problem arises also to the dependability of gate dielectric film etc. Hereafter, this problem is explained.

[0025] In the conventional technique mentioned above, in the process of drawing 22 (h), after removing the aluminum film 513 of a P type field by wet etching, the cobalt film 515 is formed in the removed field at drawing 23 (i) and the process of (j). Therefore, by etching of the aluminum film 513 etc., the front face of gate dielectric film 512 will deteriorate, and a bad influence will arise to the dependability of gate dielectric film.

[0026]
[Problem(s) to be Solved by the Invention] As stated above, since etching advanced deeply in a longitudinal direction in case etching removal of the dummy gate is carried out, there was a problem that detailed-izing was difficult, with the conventional DAMASHIN gate technique. Moreover, there was also a problem of having a bad influence on the dependability of gate dielectric film etc., by carrying out etching removal of the dummy gate.
[0027] This invention is made to the above-mentioned conventional problem, sets it as the 1st purpose to attain detailed-ization of a semiconductor device in the semiconductor device with which a gate electrode is produced using a DAMASHIN gate technique etc., and sets it as the 2nd purpose to secure the dependability of a gate electrode etc.
[0028]
[Means for Solving the Problem] This invention (invention A) is a semiconductor device with which the gate electrode of an N type MIS transistor and each P type MIS transistor is formed through gate dielectric film in the crevice formed in the semi-conductor substrate. One [at least] gate electrode of an N type MIS transistor and a P type MIS transistor is constituted by the laminated structure of two or more metal content film. That and it is smaller than the work function (W2) of the part of the metal content film with which the work function (W1) of the part of the metal content film which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least It considers as the description.
[0029] This invention (invention B) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which removes the 1st metal content film formed in one field of the 1st or 2nd gate formation field, It consists of a process which embeds the crevice of the field of the both sides of the 1st and 2nd gate formation fields by forming the 2nd metal content film on the 1st metal content film saved to the field of another side of the 1st or 2nd gate formation field, and the gate dielectric film of one field of the 1st or 2nd gate formation field. The inside of said 1st and 2nd metal content film, The work function of the part of the metal content film of the direction where the work function (W1) of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least It is characterized by being smaller than (W2).
[0030] This invention (invention C) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which removes the 1st metal content film formed in one field of the 1st or 2nd gate formation field, The process which forms the 3rd metal content film on the 1st metal content film saved to the field of another side of the 1st or 2nd gate formation field, and the gate dielectric film of one field of the 1st or 2nd gate formation field, The process which removes the 3rd metal content film formed in the field of another side of the 1st or 2nd gate formation field, By forming the 2nd metal content film on the 1st metal content film exposed to the field of another side of the 3rd metal content film top saved to one field of the 1st or 2nd gate formation field, and the 1st or 2nd gate formation field It consists of a process which embeds the crevice of the field of the both sides of the 1st and 2nd gate formation fields. The inside of said 1st and 2nd metal content film, The work function of the part of the metal content film of the direction where the work function (W1) of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least It is characterized by being smaller than (W2).
[0031] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor is smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this invention (invention A, B, and C), the work function of the gate electrode of N type and each P type MIS transistor can be optimized, and it is possible to optimize the threshold electrical potential difference of N type and a P type MIS transistor.

[0032] Moreover, according to this invention (invention A, B, and C), since one [at least] gate electrode of an N type MIS transistor and a P type MIS transistor is formed by two or more metal content film, even if its resistivity of the film of the part which touches gate dielectric film is not low, resistance of the whole gate electrode can be made low by preparing the film with low resistivity in an upper layer side.
[0033] Moreover, according to this invention (invention B and C), since the 2nd metal content film is formed on the 1st and 3rd metal content film, thickness of the 1st and 3rd metal content film can be made thin. Therefore, in case the metal content film (the 1st, 3rd metal content film) formed in one field of the 1st or 2nd gate formation field is removed, it can prevent that etching advances deeply to the field of another side of the 1st or 2nd gate formation field, and it becomes possible to attain detailed-ization of a semiconductor device.
[0034] In addition, it is desirable that a work function W1 is in the side near [center / (one half of locations of a band gap) / of the band gap of the semi-conductor used for a semi-conductor substrate] a conduction band in this invention (invention A, B, and C), and a work function W2 is in the side near [center / of a band gap] a load electronic band. Moreover, although the thickness of the field which touches the gate dielectric film which determines the threshold of an MIS transistor should just be more than thickness from which a desired threshold is obtained, it is made to become more than 10 atomic-layer extent preferably.
[0035] Moreover, what is necessary is just to be able to change both work function by changing a presentation or the crystal structure among both in this invention (invention A, B, and C), even if each part which touches the gate dielectric film of N type and a P type MIS transistor does not necessarily need to be an ingredient of a different kind and is an ingredient of the same kind.
[0036] This invention (invention D) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, It consists of a process which changes the 1st metal content film into the 2nd metal content film by making the matter contained in the 1st metal content film formed in one field of the 1st or 2nd gate formation field, and matter other than this matter react. The inside of said 1st and 2nd metal content film, The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.
[0037] This invention (invention E) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which changes the 1st metal content film into the 2nd metal content film by making the matter contained in the 1st metal content film formed in one field of the 1st or 2nd gate formation field, and matter other than this matter react, It consists of a process which changes the 1st metal content film into the 3rd metal content film by making the matter contained in the 1st metal content film formed in the field of another side of the 1st or 2nd gate formation field, and matter other than this matter react. The inside of said 2nd and 3rd metal content film, The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.
[0038] This invention (invention F) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, It consists of a process which forms the 2nd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface. the inside of the 1st metal content film formed in one field of the 1st or 2nd gate formation field -- this -- among said 1st and 2nd metal content film The work function of the part of the metal content film of the direction which touches

the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.

[0039] This invention (invention G) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, the inside of the 1st metal content film formed in one field of the 1st or 2nd gate formation field -- this -- with the process which forms the 2nd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface It consists of a process which forms the 3rd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface. the inside of the 1st metal content film formed in the field of another side of the 1st or 2nd gate formation field -- this -- among said 2nd and 3rd metal content film The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.

[0040] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor is smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this invention (invention D, E, F, and G), the work function of the gate electrode of N type and each P type MIS transistor can be optimized, and it is possible to optimize the threshold electrical potential difference of N type and a P type MIS transistor.

[0041] Moreover, change the 1st metal content film into the 2nd and 3rd metal content film by making the matter contained in the 1st metal content film, and matter other than this matter react according to this invention (invention D, E, F, and G). Or since the 2nd and 3rd metal content film is formed by diffusing matter other than the matter contained in the 1st metal content film in the inside of the 1st metal content film, and depositing a gate-dielectric-film interface A gate electrode can be produced without etching the metal content film formed on the gate dielectric film in a crevice, and it is possible to prevent the fall of the dependability of gate dielectric film.

[0042] In addition, it is desirable that a work function W1 is in the side near [center / (one half of locations of a band gap) / of the band gap of the semi-conductor used for a semi-conductor substrate] a conduction band in this invention (invention D, E, F, and G), and a work function W2 is in the side near [center / of a band gap] a load electronic band. Moreover, although the thickness of the field which touches the gate dielectric film which determines the threshold of an MIS transistor should just be more than thickness from which a desired threshold is obtained, it is made to become more than 10 atomic-layer extent preferably.

[0043]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained with reference to a drawing.

[0044] (Operation gestalt 1) An example of the production process concerning the 1st operation gestalt of this invention is hereafter explained with reference to drawing 1 (a) - drawing 3 (i).

[0045] First, the isolation 102 of STI structure is formed on a silicon substrate 101. Then, silicon oxide 103 of about 2-6nm of thickness is formed as a dummy insulator layer removed in the future. Furthermore, the laminated structure of the polish recon film 104 of about 150nm of thickness and the silicon nitride 105 of about 50nm of thickness is formed as the dummy gate removed in the future. These dummy insulator layers and the dummy gate are formed using the usual techniques (membrane formation techniques, such as oxidation and CVD, a lithography technique, RIE technique, etc.). Then, the impurity diffused layer for extensions used as the source drain diffusion layer 106 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 104 and silicon nitride 105) as a mask. Then, a gate side-attachment-wall insulator layer with a width of face of about 20-40nm which consists of a silicon nitride 107 is formed with a CVD technique and a RIE technique (drawing 1 (a)).

[0046] Next, the high concentration impurity diffused layer used as the source drain diffusion layer 108 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 104 and silicon nitride 105) an a gate side-attachment-wall insulator layer (silicon nitriding 107) as a mask. Furthermore, the silicide film (silicide

such as cobalt or titanium) 109 with a thickness of about 40nm is formed only in a source drain field by using the dummy gate as a mask with a salicide process technique (drawing 1 (b)).
[0047] Next, silicon oxide is deposited with a CVD method as an interlayer insulation film 110. Furthermore, the front face of the silicon nitrides 105 and 107 is exposed by carrying out flattening of this interlayer insulation film 110 with a CMP technique (drawing 1 (c)).
[0048] Next, the silicon nitride 105 of the dummy gate upper part is alternatively removed to an interlayer insulation film 110, for example using phosphoric acid. At this time, the silicon nitride 107 is also etched to height extent of the polish recon film 104. Then, the etching technique using the radical of halogen atoms, such as a fluorine, removes the polish recon film 104 alternatively to an interlayer insulation film 110 and the silicon nitride 107, for example (drawing 2 (d)).
[0049] Next, a slot (crevice) 111 is formed by removing dummy silicon oxide 103 by wet etching, such as rare fluoric acid. Then, the hafnium oxide film (HfO2 film) which is a high dielectric insulator layer is formed in the whole surface as gate dielectric film. This hafnium oxide film is HfCl4. NH3 It is obtained by oxidizing the hafnium nitride which formed membranes by the spatter using the target of the used CVD method, a hafnium nitride (HfN), or a hafnium, after forming a hafnium nitride (HfN film) (drawing 2 (e)).
[0050] Next, the hafnium nitride 113 whose work function is about 4eV is desirably formed on the whole surface by 10nm or less about 10nm in thickness using a CVD method or a spatter (drawing 2 (f)).
[0051] Although the process of the above drawing 1 (a) - drawing 2 (f) was performed to the both sides of an N type MIS transistor formation field and a P type MIS transistor formation field, it showed only one field on the drawing. From future processes, the both sides of an N type MIS transistor (N type MISFET) formation field and a P type MIS transistor (P type MISFET) formation field are shown on a drawing.
[0052] It covers except a P type MIS transistor formation field by the resist 114 after the process of drawing 2 (f) using a lithography technique. The top view of the principal part at this time is typically shown in drawing 4 (a) (drawing 3 (g)).
[0053] Next, only a P type field removes the hafnium nitride 113 by performing wet etching by hydrogen peroxide solution. The top view of the principal part at this time is typically shown in drawing 4 (b). Since the hafnium oxide film 112 of gate dielectric film is insoluble to hydrogen peroxide solution, it is not etched. Moreover, since the hafnium nitride 113 is very thin (about 10nm), unlike the case of the conventional technique, the hafnium nitride 113 is not deeply etched to an N type field. that is, in this example, the thickness of the hafnium nitride 113 is about 10nm -- it comes out and the lateral amount E of etching is set to about 10nm. Therefore, if the distance D between components is about 20nm or more, the trouble of the conventional technique can be canceled and it will become possible to perform large detailed-ization (drawing 3 (h)).
[0054] Next, after removing resist 114, a work function deposits the cobalt film 115 on the whole surface as noble-metals film which is about 5eV. Membrane formation of cobalt is performed using a spatter, or they are Co (CO)4 and Co2. 8, CoF2, and CoCl2 Or CoBr2 It carries out using the CVD method used as the gas source. Then, with a CMP technique, flattening of the cobalt film 115, the hafnium nitride 113, and the hafnium oxide film 112 is performed until an interlayer insulation film 110 is exposed. The top view of the principal part at this time is typically shown in drawing 4 R> 4 (c) (drawing 3 (i)).
[0055] According to the above process, as gate electrode structure, N type consists of a laminated structure of the hafnium nitride 113 and the cobalt film 115, and C-MIS transistor which consists of monolayer structure of the cobalt film 115 completes P type.
[0056] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor can be made smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this operation gestalt (a work function is [the hafnium nitride 113 / a work function] about 5eV at the example mentioned above for about 4eV and the cobalt film 115), it is possible to optimize the work function of the gate electrode of N type and each P type MIS transistor, and to optimize the threshold electrical potential difference of both transistors.
[0057] Moreover, with this operation gestalt, in case the hafnium nitride 113 of a P type field is removed, since the thickness of the hafnium nitride 113 is very thin, it can avoid that the hafnium nitride 113 is deeply etched to an N type field, and it becomes possible to perform large detailed-ization. Furthermore, with this operation gestalt, since the cobalt film 115 of low resistance is formed on the hafnium nitride 113, the gate electrode of an N type MIS transistor can reconcile optimization of a work function, and low resistance-ization.
[0058] Drawing 5 shows the component separation distance (distance between components, distance D shown in drawing 4) dependency of a threshold (threshold voltage) about the N type and the P type MIS transistor by this

operation gestalt and the conventional technique.
[0059] In this operation gestalt and the conventional technique, about the P type MIS transistor, the threshold serves as [the component separation distance D] regularity and a low battery (about -0.2V) to about 400nm. On the other hand, about an N type MIS transistor, a threshold is beginning to rise [the distance D between components] by 300nm or less with the conventional technique. This is because it consists of metals a part of whose N type MIS transistors are about 5.0eV of work functions. On the other hand, with this operation gestalt, even if it makes distance D between components detailed to 40nm, it turns out that a threshold is fixed.
[0060] In the example mentioned above, the gate electrode of an N type MIS transistor explained the case where the gate electrode of a P type MIS transistor was the monolayer structure of the cobalt film, by the laminated structure of a hafnium nitride and the cobalt film. Not only gate electrode structure such but various deformation is possible for this operation gestalt. Then, some modifications are explained below.
[0061] the fundamental gate structure in this operation gestalt -- three kinds, Structure A, Structure B, and Structure C, -- it is . About Structure A, drawing 7 corresponds about Structure B and drawing 8 corresponds [drawing 6 / Structure / C], respectively. About such structures A, Structure B, and Structure C, structure (it considers as Structure D) as shown in drawing 9 is also included as a variation of such structures. In addition, drawing 6 - drawing 9 show only gate dielectric film and a gate electrode typically.
[0062] The gate electrode of an N type MIS transistor consists of the 1st metal content film F1 and the 2nd metal content film F2 which were formed on gate dielectric film F0, the gate electrode of a P type MIS transistor consists of the 2nd metal content film F2 formed on gate dielectric film F0, and Structure A (refer to drawing 6) has the work function of the 1st metal content film F1 smaller than the work function of the 2nd metal content film F2.
[0063] The process at which the manufacture approach of Structure A forms the 1st metal content film F1 on the gate dielectric film F0 of the gate formation field of the both sides for N type and P type MIS transistors, The process which removes the 1st metal content film F1 of the gate formation field for P type MIS transistors, By forming the 2nd metal content film F2 on the 1st [of the gate formation field for N type MIS transistors] metal content film F1, and the gate dielectric film F0 of the gate formation field for P type MIS transistors It consists of a process which embeds the crevice of the gate formation field of the both sides of N type and a P type MIS transistor.
[0064] The gate electrode of a P type MIS transistor consists of the 1st metal content film F1 and the 2nd metal content film F2 which were formed on gate dielectric film F0, the gate electrode of an N type MIS transistor consists of the 2nd metal content film F2 formed on gate dielectric film F0, and the work function of structure of the 1st metal content film F1 is [B (refer to drawing 7)] smaller than the work function of the 2nd metal content film F2.
[0065] The process at which the manufacture approach of Structure B forms the 1st metal content film F1 on the gate dielectric film F0 of the gate formation field of the both sides for N type and P type MIS transistors, The process which removes the 1st metal content film F1 of the gate formation field for N type MIS transistors, By forming the 2nd metal content film F2 on the 1st [of the gate formation field for P type MIS transistors] metal content film F1, and the gate dielectric film F0 of the gate formation field for N type MIS transistors It consists of a process which embeds the crevice of the gate formation field of the both sides of N type and a P type MIS transistor.
[0066] It is as drawing 1 - drawing 3 R> 3 having shown the concrete example of Structure A. Moreover, about Structure B, most manufacture approaches shown in drawing 1 - drawing 3 can be diverted (the thing suitable for Structure B is used for each component). Main changed parts are points which carry out the mask of the P type MIS transistor field by the resist instead of an N type MIS transistor field in the process of drawing 3 (g).
[0067] Structure C (refer to drawing 8) consists of the 1st metal content film F1 and the 2nd metal content film F2 with which the gate electrode of an N type MIS transistor was formed on gate dielectric film F0. The gate electrode of a P type MIS transistor consists of the 3rd metal content film F3 and the 2nd metal content film F2 which were formed on gate dielectric film F0, and the work function of the 1st metal content film F1 is smaller than the work function of the 3rd metal content film F3.
[0068] The process at which the manufacture approach of Structure C forms the 1st metal content film F1 on the gate dielectric film F0 of the gate formation field of the both sides for (refer to drawing 10), N type, and P type MIS transistors, The process which removes the 1st metal content film F1 of the gate formation field for P type MIS transistors, The process which forms the 3rd metal content film F3 on the 1st [of the gate formation field for N type MIS transistors] metal content film F1, and the gate dielectric film F0 of the gate formation field

for P type MIS transistors, The process which removes the 3rd metal content film F3 of the gate formation field for N type MIS transistors, By forming the 2nd metal content film F2 on the 1st [of the gate formation field for N type MIS transistors] metal content film F1, and the 3rd [of the gate formation field for P type MIS transistors] metal content film F3 It consists of a process which embeds the crevice of the gate formation field of the both sides of N type and a P type MIS transistor.

[0069] In addition, the structure (structure D) where the 2nd metal content film F2 is two or more kinds of cascade screens is also included in Structure A, Structure B, and Structure C. Corresponding to the example of drawing 6 , the 2nd metal content film F2 of N type and a P type MIS transistor is constituted from an example of drawing 9 by the cascade screen of metal content film F2a and F2b.

[0070] Hereafter, the structure A mentioned above - Structure D are explained further.

[0071] (1) In Structure A (refer to drawing 6), the 2nd metal content film F2 is used as a barrier metal which determines the threshold of a P type MIS transistor, respectively as a barrier metal the 1st metal content film F1 decides the threshold of an N type MIS transistor to be.

[0072] What has possible performing etching (wet etching or dry etching by the radical atom or the radical molecule) which has the work function (4.6eV or less, desirably about 4eV) which can optimize the threshold of an N type MIS transistor, and does not have a damage is used for the 1st metal content film F1. HfN and ZrN are raised to a typical ingredient. These are expected that a work function is about 4eV, and are suitable as a barrier metal of N type.

[0073] What has the low resistivity which has the work function (4.6eV or more, desirably about 5eV) which can optimize the threshold of a P type MIS transistor, and can carry out [low ****]-izing of the gate electrode is used for the 2nd metal content film F2. The ingredient of a noble-metals system has many whose work function is about 5eV, and fits the 2nd metal content film. For Co, from a viewpoint of resistivity, about 5micro ohm-cm and nickel are [about 6micro ohm-cm and Pt] about 10micro ohm-cm. W and CoSi2 which are used as a current gate electrode Resistivity is about 5micro ohm-cm and about 20micro ohm-cm, respectively, and Co, nickel and Pt, especially Co are suitable as an ingredient of the 2nd metal content film.

[0074] It is HfO2 when barrier metal is HfN, although not limited especially about gate dielectric film F0. Using is desirable. HfN and HfO2 It is because thermal reaction cannot occur easily in an interface.

[0075] (2) In Structure B (refer to drawing 7), the 2nd metal content film F2 is used as a barrier metal which determines the threshold of an N type MIS transistor, respectively as a barrier metal the 1st metal content film F1 decides the threshold of a P type MIS transistor to be.

[0076] What has possible performing etching (wet etching or dry etching by the radical atom or the radical molecule) which has the work function (4.6eV or more, desirably about 5eV) which can optimize the threshold of a P type MIS transistor, and does not have a damage is used for the 1st metal content film F1. In a typical ingredient, it is WNx. And WSix Ny It is raised.

[0077] What has the low resistivity which has the work function (4.6eV or less, desirably about 4eV) which can optimize the threshold of an N type MIS transistor, and can carry out [low ****]-izing of the gate electrode is used for the 2nd metal content film F2. aluminum (or alloy containing aluminum) is raised as a typical ingredient.

[0078] (3) In Structure C (refer to drawing 8), as a barrier metal the 1st metal content film F1 decides the threshold of an N type MIS transistor to be, the 3rd metal content film F3 is used as a barrier metal which determines the threshold of a P type MIS transistor, respectively, and the 2nd metal content film F2 is used as an electrode material of low resistance.

[0079] what has possible performing etching (wet etching or dry etching by the radical atom or the radical molecule) which has the work function (4.6eV or less, desirably about 4eV) which can optimize the threshold of an N type MIS transistor on the 1st metal content film F1, and does not have a damage in it -- HfN is used typically. what has possible performing etching which has the work function (4.6eV or more, desirably about 5eV) which can optimize the threshold of a P type MIS transistor on the 3rd metal content film F3, and does not have a damage in it -- typical -- WNx It uses. aluminum (or alloy containing aluminum) is used for the 2nd metal content film F2 at the ingredient and representation target which are low resistance.

[0080] (4) With the structure A in Structure D (refer to drawing 9), or the structure corresponding to Structure B As 2nd metal content film F2 which is a cascade screen, it is the work function (about N type, 4.6eV or less) which can optimize the threshold of N type or a P type MIS transistor about film F2a by the side of a lower layer. About 4eV and P type, it is called for desirably that it is [4.6eV or more] low resistance to have 5eV desirably at film F2b by the side of the upper layer.

[0081] With the structure corresponding to the structure C in Structure D, although there is no merit of using the

film by the side of the lower layer of the 2nd metal content film in order to optimize the threshold of a transistor since the 1st metal content film F1 and the 3rd metal content film F3 are under the 2nd metal content film F2, there is a merit that diffusion of the metal to the gate dielectric film from an upper layer side can be controlled.
[0082] Typically, it structure D Sets and the thing corresponding to Structure A which constituted [the 1st metal content film F1] upper layer side F2b of RuO2 and the 2nd metal content film for lower layer side F2a of HfN and the 2nd metal content film from aluminum is raised.
[0083] (5) In Structure A, Structure B, and Structure C, it is desirable to use for the 1st metal content film F1 the metallic compounds which are conductors. As a barrier metal for N type MIS transistors, a hafnium nitride, a zirconium nitride, a titanium nitride, a tantalum nitride, a tantalum nitride, and a niobium nitride are raised. A tungsten nitride and a tungsten silicification nitride are raised as a barrier metal for P type MIS transistors.
[0084] (6) In Structure A and Structure C, it is desirable to use the film which contains the alloy containing platinum, palladium, nickel, cobalt, a rhodium, a ruthenium, a rhenium, iridium, gold, silver, copper, or these metals in the 2nd metal content film F2.
[0085] (7) In Structure A, Structure B, and Structure C, it is desirable to use for the 2nd metal content film F2 the film containing the metallic compounds which are conductors.
[0086] As metallic compounds, a metallic oxide (ruthenium oxide, an iridium acid ghost, rhenium oxide, platinum oxide, rhodium oxide) is raised [1st]. Noble-metals system oxide is a conductor in many cases, and is for being easy to obtain the work function suitable for a P type MIS transistor.
[0087] As metallic compounds, metal silicide (platinum silicide, palladium silicide, nickel silicide) is raised to the 2nd. These can obtain the work function suitable for N type or a P type MIS transistor (especially P type MIS transistor).
[0088] As metallic compounds, a metal nitride (a hafnium nitride, a zirconium nitride, a titanium nitride, a tantalum nitride, niobium nitride) is raised to the 3rd. These can obtain the work function suitable for an N type MIS transistor.
[0089] (8) In Structure D, it is desirable for the film of the lowest layer to be [of the 2nd metal content film F2] metallic compounds at least. As metallic compounds, a metallic oxide (ruthenium oxide, an iridium acid ghost, rhenium oxide, platinum oxide, rhodium oxide), metal silicide (platinum silicide, palladium silicide, nickel silicide), a metal nitride (a hafnium nitride, a zirconium nitride, a titanium nitride, a tantalum nitride, a niobium nitride, a tungsten nitride, tungsten nitride), and tungsten nitriding silicide are raised.
[0090] (9) In Structure C, it is desirable to use a tungsten nitride or tungsten nitriding silicide for the 3rd metal content film F3.
[0091] In Structure A - Structure D (10) As gate dielectric film F0 HfO2, ZrO2, TiO2, a silicon nitride, and aluminum 2O3, The zirconic acid-ized film containing Ta 2O5, Nb 2O5, Y2 O3, CeO2, and an yttrium, the compound film of barium, strontium, titanium, and oxygen, the compound film of lead, a zirconium, titanium, and oxygen, and silicon oxide are raised.
[0092] By the method of forming the zirconic acid-ized film containing HfO2, ZrO2, TiO2, Ta 2O5, Nb 2O5, Y2 O3, CeO2, and an yttrium It is HfCl4, ZrCl4, TiCl4, TaCl5, NbCl5, and Y(Thd) 3 (here, Thd is 2, 2, 6, and 6-tetramethyl - 3 and 5-hepta-screw ONETO is meant.), respectively. Ce (Thd)4 and Zr4 (Thd) Y(Thd) 3 To mixed gas, it is O2. There is the approach of forming membranes directly with the CVD method which mixed gas.
[0093] O2 [moreover,] instead of [of gas] -- for example, NH3 etc. -- it uses, the zirconium nitride which contains each metal nitride, i.e., HfN, ZrN, TiN, TaN, NbN, YN, and CeN, and an yttrium first is formed, and it may be made to use each metal nitride by thermal oxidation as an oxide after that. When using this thermal oxidation approach, it is desirable to oxidize thermally a nitride 5nm or less, or to make it repeat nitride deposition / oxidation of 5nm or less two or more times so that nitrogen may not remain in the film. When a thick nitride is oxidized thermally and oxidation temperature is low temperature 500 degrees C or less, it is because it was found out that it becomes impossible for the nitrogen which is a product from the layer which newly oxidized to escape from the interior of membranous outside, and it remains in the film.
[0094] Moreover, before forming the metallic oxide mentioned above, the gate dielectric film F0 of a laminated structure may be produced by forming the silicon nitride by the oxidation nitride using oxidation in the silicon oxide by thermal oxidation, and NO gas etc., or the CVD method on a silicon substrate, and forming the metal oxide film mentioned above after that.
[0095] (11) As film by the side of the lowest layer of a gate electrode, when using HfN, ZrN, and TiN, hydrogen peroxide solution can be used for these etching. It is required not to etch gate dielectric film F0 at the time of etching using this hydrogen peroxide solution. HfO2 mentioned above as gate dielectric film F0, ZrO2, TiO2, and

Si3 N4, aluminum 2O3, Ta 2O5, Nb 2O5, and Y2 O3, Since these are insoluble to hydrogen peroxide solution when using the zirconic acid-ized film containing CeO2 and an yttrium, the compound film of barium, strontium, titanium, and oxygen, the compound film of lead, a zirconium, titanium, and oxygen, and silicon oxide, a problem is not produced.

[0096] As film by the side of the lowest layer of a gate electrode, when using TaN and NbN, these are meltable into the mixed liquor of a hydrochloric acid and a nitric acid. Therefore, what is necessary is just to use for gate dielectric film F0 silicon oxy-night RAIDO which contains insoluble HfO2, ZrO2, TiO2, Si3 N4, silicon oxide, and nitrogen 1% or more into this mixed liquor.

[0097] When using aluminum as film by the side of the lowest layer of a gate electrode, aluminum is meltable into the mixed liquor of phosphoric acid and a nitric acid. Therefore, what is necessary is just to use the zirconic acid-ized film which contains insoluble HfO2, ZrO2, TiO2, Ta 2O5, Nb 2O5, and an yttrium in gate dielectric film F0 at this mixed liquor, the compound film of barium, strontium, titanium, and oxygen, the compound film of lead, a zirconium, titanium, and oxygen, and silicon oxide.

[0098] (12) When the metal nitride (HfN, ZrN, TiN, TaN, NbN) mentioned above as film by the side of the lowest layer of a gate electrode is used, as for how of the metal nitride film and gate dielectric film to combine, it is desirable to fulfill the following conditions other than the etching resistance mentioned above. That is, it is made for the free energy of Gibbs of the metallic oxide which consists of a metallic element which constitutes a metal nitride to become below the free energy of Gibbs of the metal oxide film used for gate dielectric film, or silicon oxide. When it does in this way, it is for possibility that a metal nitride will return gate dielectric film to decrease. Specifically, gate dielectric film is HfO2. It is desirable to use HfN, ZrN, TiN, TaN, and NbN for a case as a metal nitride, and gate dielectric film is Ta 2O5. It is desirable to use TaN and NbN for a case as a metal nitride.

[0099] (Operation gestalt 2) An example of the production process concerning the 2nd operation gestalt of this invention is hereafter explained with reference to drawing 11 (a) - Fig. 1414 (l).

[0100] First, the front face of a silicon substrate 201 is oxidized thermally, and silicon oxide 202 is formed. Then, the silicon nitride 203 is formed on silicon oxide 202 using a CVD method (drawing 11 (a)).

[0101] Next, the pattern of a photoresist 204 is formed on the silicon nitride 203. Then, an isolation slot is formed by using this resist pattern 204 as a mask, and carrying out patterning of the silicon nitride 203, silicon oxide 202, and the silicon substrate 201 using anisotropic etching (drawing 11 (b)).

[0102] Next, a photoresist 204 is ashed and removed. Then, it is the front face of the exposed isolation slot 950 degrees C and HCl/O2 Silicon oxide 205 is formed by oxidizing thermally in an ambient atmosphere. Then, silicon oxide 206 is deposited on the whole surface using a CVD method, and an isolation slot is embedded. Furthermore, it grinds until the front face of the silicon nitride 203 exposes silicon oxide 206 using the CMP method (drawing 11 (c)).

[0103] Next, the silicon nitride 203 is alternatively removed using heat phosphoric acid. Then, silicon oxide 202 is removed using a rare fluoric acid solution. In this case, the upside silicon oxide 206 and the silicon oxide 205 of an isolation slot are etched somewhat, and the front face of the silicon substrate 201 near the up edge of an isolation slot is exposed (drawing 12 (d)).

[0104] Next, 900 degrees C and HCl/O2 It oxidizes thermally in an ambient atmosphere and the silicon oxide 207 used as a dummy insulator layer is formed. Since the dummy insulator layer 207 is formed not only an MIS transistor formation field top but on the up edge of an isolation slot, the exposure of a silicon substrate of it is lost (drawing 12 (e)).

[0105] Next, after forming the polish recon film 208 in the whole surface, the dummy gate is formed by carrying out patterning of this polish recon film 208 (drawing 12 (f)).

[0106] Next, the dummy gate which consists of polish recon film 208 is used as a mask, and impurity ion is injected into the front face of a silicon substrate 201. Furthermore, the source drain diffusion layer 209 is formed in self align to the dummy gate by performing hot annealing treatment. Then, an interlayer insulation film 210 is deposited on the whole surface, and flattening is carried out until the polish recon film 208 exposes this interlayer insulation film 210 using the CMP method. Then, it is the exposed polish recon film 208 CF4 / O2 The downflow technique using gas removes (drawing 13 (g)).

[0107] Next, in order to adjust the threshold electrical potential difference of N type and each P type MIS transistor, the impurity of N type and P type is introduced with ion-implantation into a silicon substrate 201 through the exposed dummy insulator layer 207, respectively. Then, a slot (crevice) 211 is formed by removing the dummy insulator layer 207 using a rare fluoric acid solution. Then, it is Ta 2O5 as gate dielectric film. The film 212 is formed. Furthermore, the ruthenium (Ru) film or the palladium (Pd) film 213 is formed about 10nm of

thickness as a gate electrode material of a P type MIS transistor (drawing 13 R> 3 (h)).
[0108] Next, the silicon nitride 214 is formed in the whole surface by 10nm thickness by the plasma-CVD method. This silicon nitride 214 is used as diffusion prevention film for preventing diffusion of the indium (In) or tin (Sn) formed at a next process. Then, the pattern of a photoresist 215 is formed on a P type MIS transistor field (drawing 13 (i)).
[0109] Next, the silicon nitride 214 of the exposed N type MIS transistor field is removed using the downflow method. a photoresist 215 -- ashing -- after processing removes, the indium (In) film or the tin (Sn) film is formed in the whole surface by 1-2nm thickness as a gate electrode material of an N type MIS transistor (drawing 14 (j)).
[0110] Next, inside [of 200 degrees C - about 400 degrees C] low-temperature annealing is performed. Since the silicon nitride 214 is formed in the P type MIS transistor field, an indium or tin is alternatively spread only to an N type MIS transistor field by this annealing treatment. An indium or tin is diffused through the grain boundary of the ruthenium film or the palladium film 213. Ta 2O5 from which an indium or tin serves as gate dielectric film by this It deposits in an interface with the film 212, the ruthenium film, or the palladium film 213. Consequently, the indium film or the tin film 216 used as the gate electrode of an N type MIS transistor is formed (drawing 14 (k)).
[0111] Next, the indium film or the tin film 216 on a P type MIS transistor field is removed alternatively, and the silicon nitride 214 is further removed using the downflow method. Then, the tungsten film 217 is embedded in the slot of the gate electrode field of N type and a P type MIS transistor. furthermore, the CMP method -- using -- the ruthenium film outside a slot or the palladium film 213, the indium film or the tin film 216, and Ta 2O5 The film 212 and the tungsten film 217 are removed, and it leaves only Mizouchi the tungsten film 217. Thereby, the gate electrode with which the indium film or the tin film 216 was formed in the lowest layer for the gate electrode with which the ruthenium film or the palladium film 213 was formed in the lowest layer with the N type MIS transistor consists of P type MIS transistors. Henceforth, an interlayer insulation film 218 and wiring 219 grade are formed, and a semiconductor integrated circuit is completed (drawing 14 (l)).
[0112] In addition, the metal M1 (in the example mentioned above) which constitutes the gate electrode of a P type MIS transistor from an example mentioned above Although it was made to deposit a metal M2 in the gate-dielectric-film interface of an N type MIS transistor by diffusing the metal M2 (the example mentioned above an indium or tin) which constitutes the gate electrode of an N type MIS transistor for the inside of a ruthenium or palladium The alloy of a metal M1 and a metal M2 is formed, and you may make it this alloy constitute the gate electrode of an N type MIS transistor by diffusing a metal M2 in a metal M1 (it considers as a modification 1).
[0113] Moreover, in case the metal M2 which constitutes the gate electrode of an N type MIS transistor for the inside of the metal M1 which constitutes the gate electrode of a P type MIS transistor from an example mentioned above is diffused Although it was made to make an N type MIS transistor field diffuse a metal M2 alternatively by using as a mask of diffusion of the silicon nitride 214 The silicon nitride 214 forms a metal M2 alternatively only on the metal M1 of an N type MIS transistor field, and you may make it diffuse a metal M2 in a metal M1 alternatively only in an N type MIS transistor field like the example mentioned above, without forming (it considers as a modification 2).
[0114] Furthermore, although the basic example and modifications 1 and 2 which were mentioned above deposit a metal M2 in a gate-dielectric-film interface or are performing the approach of forming the alloy of a metal M1 and a metal M2, to the gate electrode of an N type MIS transistor, they may perform the same approach to the gate electrode of a P type MIS transistor.
[0115] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor can be made smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this operation gestalt, it is possible to optimize the work function of the gate electrode of N type and each P type MIS transistor, and to optimize the threshold electrical potential difference of both transistors. Moreover, since etching removal of the metal membrane formed in Mizouchi for gate electrode formation is not carried out like before with this operation gestalt, it is possible to control the fall of the dependability of gate dielectric film.
[0116] (Operation gestalt 3) An example of the production process is hereafter explained with reference to drawing 1515 (a) - drawing 17 (h) about the 1st example concerning the 3rd operation gestalt of this invention.
[0117] first, a silicon substrate 301 top -- isolation 302 -- forming -- then, an N type MIS transistor field -- the well of P type -- a diffusion layer 303 -- a P type MIS transistor field -- the well of N type -- a diffusion layer 304 is formed (drawing 15 (a))

Next, about 5nm oxidizes the front face of the exposed silicon substrate 301, and the silicon oxide 305 used as a dummy insulator layer is formed. Then, the polish recon film 306 used as the dummy gate is deposited, and patterning of this is carried out to the configuration of a gate electrode. Then, the poly SHIRIKO film 306 used as the dummy gate is used as a mask, arsenic is made an N type field, the ion implantation of the boron is made to a P type field, and the shallow impurity diffused layer used as the source drain diffusion layer 307 is formed. Then, the silicon nitride 308 is deposited and a side-attachment-wall insulator layer is formed by carrying out anisotropic etching of this. Then, this side-attachment-wall insulator layer 308 and the polish recon film 306 are used as a mask, arsenic is made an N type field, the ion implantation of the boron is made to a P type field, and the deep impurity diffused layer used as the source drain diffusion layer 309 is formed (drawing 15 (b)).

[0118] Next, silicon oxide is deposited on the whole surface as an interlayer insulation film 310. Then, using the CMP method, flattening is carried out until the polish recon film 306 exposes silicon oxide 310 (drawing 15 (c)).

[0119] Next, the polish recon film 306 is removed using isotropic etching techniques, such as chemical dry etching. Then, etching removal of the exposed silicon oxide 305 is carried out by rare hydrofluoric acid treatment etc., and the slot 311 for gate electrode formation is formed in the both sides of N type and a P type MIS transistor field (drawing 16 (d)).

[0120] Next, the silicon substrate 301 of slot 311 pars basilaris ossis occipitalis for gate electrode formation is oxidized by thermal oxidation processing, and the gate dielectric film which consists of silicon oxide 312 is formed. Then, the tungsten silicide (WSi2) film 313 is deposited on the whole surface with a CVD method as a gate electrode material of an N type MIS transistor. Then, the tungsten silicide film 313 deposited on the exterior of the slot 311 for gate electrode formation by the CMP method is removed, and the tungsten silicide film 313 is made to save only in the slot 311 for gate electrode formation (drawing 16 (e)).

[0121] Next, the silicon nitride 314 is deposited on the whole surface, and only an N type MIS transistor field is made to save the silicon nitride 15 with photolithography and an etching technique further. Then, the palladium (Pd) film 315 is deposited on the whole surface by a spatter etc. (drawing 16 (f)).

[0122] Next, 600 degrees C and 1-minute room [about] annealing treatment are performed. Thereby, the tungsten silicide film 313 currently embedded at the gate electrode section of a P type MIS transistor field reacts with the palladium film 315. Consequently, the palladium silicide (Pd2 Si) film 316 is formed in the field to which the tungsten silicide film 313 existed from the first, and a tungsten is discharged in the palladium film of the upper part of this palladium silicide film 316. In an N type MIS transistor field, since it is formed silicon nitride 314, the tungsten silicide film 313 is not permuted by the palladium silicide film 316. Then, CMP etc. removes the metal and the silicon nitride 314 which remained in the exterior of the slot for gate electrode formation. Thereby, the gate electrode of a P type MIS transistor is formed with the palladium silicide film 316 (drawing 17 (g)).

[0123] Next, the silicon oxide used as an interlayer insulation film 317 is deposited on the whole surface. Then, the hole for the contact which reaches the source drain and gate electrode of an MIS transistor is formed in interlayer insulation films 317 and 310. Then, the metal membrane for wiring 318 is deposited and the MIS transistor transistor of N type and P type is completed by carrying out patterning of this (drawing 17 (h)).

[0124] In addition, although the tungsten silicide (WSi2) film was used as a gate electrode material of an N type MIS transistor in the example mentioned above, it is also possible to use silicide, such as molybdenum silicide (MoSi2), tantalum silicide (TaSi2), niobium silicide (NbSi2), or chromium silicide (CrSi2), instead of tungsten silicide.

[0125] Moreover, by forming the palladium (Pd) film on the tungsten silicide film of a P type MIS transistor field, and making palladium react with the tungsten silicide film by heat treatment in the example mentioned above Although tungsten silicide was permuted by palladium silicide (Pd2 Si, PdSi) It is also possible to use nickel (nickel) or platinum (Pt) instead of palladium, and to permute by silicide, such as nickel silicide (NiSi and NiSi2) or platinum silicide (Pt2 Si, PtSi).

[0126] Moreover, Ta 2O5 formed with the CVD method etc. although the silicon oxide obtained by heat treatment as gate dielectric film was used in the example (even the following examples [2nd and 3rd] are the same) mentioned above You may make it use the film.

[0127] Next, an example of the production process is explained with reference to drawing 18 (a) - Fig. 1818 (c) about the 2nd example concerning the 3rd operation gestalt of this invention.

[0128] In addition, since it is the same as that of the 1st example which the intermediate process (process of drawing 15 (a) - drawing 16 (e)) mentioned above, this example explains the process after the process of drawing 16 (e).

[0129] After the process of drawing 16 (e), after carrying out the mask of the N type MIS transistor field by the

resist 321, with ion-implantation, the ion implantation of the germanium ion (germanium+) is alternatively carried out only to the tungsten silicide film 313 of a P type MIS transistor field, and it is referred to as tungsten silicide film 313a containing germanium. At this time, concentration of the germanium ion introduced into the tungsten silicide film 313 is made into the concentration more than the solid-solution limit of the germanium in tungsten silicide (about [for example, / 1x1017cm -] 3) (drawing 18 (a)).

[0130] Next, the mask of the P type MIS transistor field is carried out by the resist 322, and with ion-implantation, the ion implantation of the indium ion (In+) is alternatively carried out only to the tungsten silicide film 313 of an N type MIS transistor field, and it is referred to as tungsten silicide film 313b containing an indium. At this time, concentration of the indium ion introduced into the tungsten silicide film 313 is made into the concentration more than the solid-solution limit of the indium in tungsten silicide (about [for example, / 1x1017cm -] 3) (drawing 18 (b)).

[0131] Next, the germanium and the indium which were poured in into the tungsten silicide film 313 deposit in the interface of the tungsten silicide film 313 and the silicon oxide 312 which is gate dielectric film by performing 800 degrees C and heat treatment for about 1 minute. Consequently, in a P type MIS transistor, a gate electrode is formed of the laminated structure of the germanium film 323 and the tungsten silicide film 313, and a gate electrode is formed in an N type MIS transistor of the laminated structure of the indium film 324 and the tungsten silicide film 313 (drawing 18 (c)).

[0132] Finally, the MIS transistor of N type and P type is completed like the 1st example by depositing an interlayer insulation film, making the hole for contact, and forming wiring further.

[0133] In addition, although the tungsten silicide (WSi2) film was used in the example mentioned above as an ingredient beforehand formed into the slot for gate electrodes, it is also possible to use molybdenum silicide (MoSi2), tantalum silicide (TaSi2), niobium silicide (NbSi2), or chromium silicide (CrSi2) instead of tungsten silicide.

[0134] Moreover, although the indium (In) was used with germanium (germanium) and an N type MIS transistor with the P type MIS transistor, a suitable ingredient is chosen out of germanium, an indium, antimony (Sb), platinum (Pt), palladium (Pd), etc., and you may make it deposit a separate ingredient with both the transistors of P type and N type in the example mentioned above as an ingredient which deposits a gate-dielectric-film interface. Moreover, these ingredients are deposited only about one transistor of P type or N type (it is a deed about an ion implantation only about one transistor), and you may make it use a gate electrode material (the example mentioned above tungsten silicide) from the first as a gate electrode as it is with the transistor of another side.

[0135] Furthermore, although it was made to deposit the matter which carried out the ion implantation in a gate-dielectric-film interface by heat treatment in the example mentioned above, the reactant of each matter which carried out the ion implantation of the separate matter to the gate electrode field of P type and an N type MIS transistor, and carried out the ion implantation by heat treatment etc., and the gate electrode material currently formed in the gate electrode field from the first is formed, and you may make it the work function of the reactant of an N type MIS transistor become smaller than the work function of the reactant of a P type MIS transistor.

[0136] Next, an example of the production process is explained with reference to drawing 19 (a) - Fig. 1919 (c) about the 3rd example concerning the 3rd operation gestalt of this invention.

[0137] In addition, since it is the same as that of the 1st example which the intermediate process (process of drawing 15 (a) - drawing 16 (d)) mentioned above, this example explains the process after the process of drawing 16 (d).

[0138] After the process of drawing 16 (e), a spatter and the CMP method are used for the slot for gate electrode formation, and the nickel (nickel) film 331 is embedded as a gate electrode material of a P type MIS transistor in it (drawing 19 (a)).

[0139] Next, after depositing the amorphous silicon (a-Si) film 332 on the whole surface by a spatter etc., the amorphous silicon film 332 of fields other than on an N type MIS transistor field is removed using the photolithography method, the dry etching method, etc. (drawing 19 (b)).

[0140] Next, by adding 400 degrees C and heat treatment for about 1 minute, in the gate electrode section of an N type MIS transistor field, the nickel film 331 and the amorphous silicon film 332 are made to react, and the nickel silicide (NiSi) film 333 is formed. Then, isotropic etching, such as chemical dry etching, removes the amorphous silicon film 332 which was not contributed to a reaction. Thus, by changing the nickel film 331 to the nickel silicide film 333, the work function of an ingredient can be reduced to about 4.36eV from about 5.0eV (drawing 19 (c)).

[0141] Finally, the MIS transistor transistor of N type and P type is completed like the 1st example by depositing an interlayer insulation film, making the hole for contact, and forming wiring further.
[0142] In addition, in the example mentioned above, the gate electrode of a P type MIS transistor may be formed by cobalt (Co), cobalt silicide (CoSi2), chromium (Cr) and chromium silicide (CrSi2), molybdenum (Mo), molybdenum silicide (MoSi2), etc., although nickel (nickel) and the gate electrode of an N type MIS transistor were made into nickel silicide (NiSi and NiSi2).
[0143] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor can be made smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this operation gestalt, it is possible to optimize the work function of the gate electrode of N type and each P type MIS transistor, and to optimize the threshold electrical potential difference of both transistors. Moreover, since etching removal of the metal membrane formed in Mizouchi for gate electrode formation is not carried out like before with this operation gestalt, it is possible to control the fall of the dependability of gate dielectric film.
[0144] As mentioned above, although the operation gestalt of this invention was explained, it is possible for this invention to deform within limits which are not limited to the above-mentioned operation gestalt and do not deviate from the meaning variously, and to carry out.
[0145]
[Effect of the Invention] According to this invention, it is possible by optimizing the work function of the gate electrode of N type and each P type MIS transistor to optimize the threshold electrical potential difference of N type and a P type MIS transistor. Moreover, it becomes it is possible to attain detailed-izing of a semiconductor device and low resistance-ization, and possible to raise the dependability of a gate electrode etc. further.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to amelioration of the gate electrode of a semiconductor device and its manufacture approach especially an N type MIS transistor, and a P type MIS transistor.

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PRIOR ART

[Description of the Prior Art] For high-performance-izing of an MIS transistor, detailed-izing of a component is indispensable. However, since the silicon oxide used as gate dielectric film now has the low dielectric constant, it has the problem that capacity of gate dielectric film cannot be enlarged. Moreover, since the polish recon used as a gate electrode has high resistivity, it has the problem that low resistance-ization cannot be attained. The proposal of using a metallic material for a gate electrode is made by gate dielectric film to each problem using high dielectric materials.
[0003] However, these ingredients have the fault that it is inferior to thermal resistance compared with the ingredient used now. Then, after performing an elevated-temperature process, the DAMASHIN gate technique is proposed as a technique which can form gate dielectric film and a gate electrode.
[0004] A DAMASHIN gate technique embeds an electrode material to the field which removed the dummy gate after forming in the gate formation schedule field the gate which serves as a dummy beforehand and forming a source drain diffusion layer, and removed the dummy gate, and produces a gate electrode.
[0005] Since the work function of the gate electrode of both transistors cannot be changed if the same metal is used for the gate electrode of N type and a P type MIS transistor when producing a gate electrode using a pellet scene gate technique, the threshold of N type and each P type MIS transistor cannot be rationalized.
[0006] Therefore, the manufacture process using a different gate electrode material is needed with an N type MIS transistor and a P type MIS transistor. Hereafter, an example of such a manufacture process is explained with reference to drawing 20 (a) - drawing 23 (i).
[0007] First, the isolation 502 of STI structure is formed on a silicon substrate 501. Then, silicon oxide 503 of about 6nm of thickness is formed as a dummy insulator layer removed in the future. Furthermore, the laminated structure of the polish recon film 504 of about 150nm of thickness and the silicon nitride 505 of about 50nm of thickness is formed as the dummy gate removed in the future. These dummy insulator layers and the dummy gate are formed using the usual techniques (membrane formation techniques, such as oxidation and CVD, a lithography technique, RIE technique, etc.). Then, the impurity diffused layer for extensions used as the source drain diffusion layer 506 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 504 and silicon nitride 505) as a mask. Then, a gate side-attachment-wall insulator layer with a width of face of about 40nm which consists of a silicon nitride 507 is formed with a CVD technique and a RIE technique (drawing 20 (a)).
[0008] Next, the high concentration impurity diffused layer used as the source drain diffusion layer 508 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 504 and silicon nitride 505) and a gate side-attachment-wall insulator layer (silicon nitriding 507) as a mask. Furthermore, the silicide film (silicide such as cobalt or titanium) 509 with a thickness of about 40nm is formed only in a source drain field by using the dummy gate as a mask with a salicide process technique (drawing 20 (b)).
[0009] Next, silicon oxide is deposited with a CVD method as an interlayer insulation film 510. Furthermore, the front face of the silicon nitrides 505 and 507 is exposed by carrying out flattening of this interlayer insulation film 510 with a CMP technique (drawing 20 (c)).
[0010] Next, the silicon nitride 505 of the dummy gate upper part is alternatively removed to an interlayer insulation film 510, for example using phosphoric acid. At this time, the silicon nitride 507 is also etched to height extent of the polish recon film 504. Then, the etching technique using the radical of halogen atoms, such as a fluorine, removes the polish recon film 504 alternatively to an interlayer insulation film 510 and the silicon nitride 507, for example (drawing 21 (d)).
[0011] Next, a slot (crevice) is formed by removing dummy silicon oxide 503 by wet etching, such as fluoric acid.

Then, Ta 2O5 which is a high dielectric insulator layer as gate dielectric film The film 512 is formed with a CVD method etc. Then, the aluminum film 513 is deposited as a gate electrode (drawing 21 R> 1 (e)).
[0012] Next, a CMP technique is used and it is Ta 2O5. Flattening of the film 512 and the aluminum film 513 is performed until an interlayer insulation film 510 is exposed (drawing 21 (f)).
[0013] Although the process of the above drawing 20 (a) - drawing 21 (f) was performed to the both sides of an N type MIS transistor formation field and a P type MIS transistor formation field, it showed only one field on the drawing. From future processes, the both sides of an N type MIS transistor (N type MISFET) formation field and a P type MIS transistor (P type MISFET) formation field are shown on a drawing.
[0014] It covers except a P type MIS transistor formation field by the resist 514 after the process of drawing 21 (f) using a lithography technique (drawing 22 (g)).
[0015] Next, only a P type field removes the aluminum film 513 by performing wet etching by phosphoric acid. Although the silicon nitride 507 is exposed at this time, in the phosphoric acid of a room temperature, it is hardly etched (drawing 22 R> 2 (h)).
[0016] Next, after removing a resist 514, the cobalt film 515 is deposited on the whole surface as a metal with which a work function is set to about 5eV (drawing 23 (i)).
[0017] Next, using a CMP technique, flattening of the cobalt film 515 is performed until an interlayer insulation film 510 is exposed (drawing 23 (j)).
[0018] According to the above process, as gate electrode structure, N type consists of aluminum film 513, and C-MIS transistor which consists of cobalt film 515 completes P type. Since a work function is about 5eV, it is with an N type MIS transistor and a P type MIS transistor, and, as for about 4.2eV and the cobalt film 515, can optimize the work function of a gate electrode by each, and as for the aluminum film 513, a work function can optimize the threshold electrical potential difference of both transistors.
[0019] However, with the conventional technique mentioned above, a big problem arises to detailed-izing. Hereafter, this problem is explained.
[0020] Drawing 24 (a), drawing 24 (b), and drawing 24 (c) are the top views having shown typically the principal part in drawing 22 (g), drawing 22 (h), and drawing 2323 (j), respectively. The distance between each source drain of an N type MIS transistor and a P type MIS transistor, i.e., the distance between components, is set to D.
[0021] In the process of drawing 22 (h), if a resist 514 is used as a mask and wet etching of the aluminum film 513 of a P type field is carried out, wet etching will advance isotropic. Therefore, etching will go deeply to the field by which the mask was carried out by the resist 514, and as shown in drawing 24 (b), the aluminum film 513 will be etched to an N type field.
[0022] Therefore, the completed transistor structure comes to be shown in drawing 24 (c). That is, a gate electrode will be constituted from an N type field by the aluminum film and cobalt film with which work functions differ mutually. The field where thresholds differ will exist and it becomes impossible therefore, to desire a setup of a low threshold electrical potential difference in an N type MIS transistor.
[0023] The problem mentioned above is examined further. The amount E of etching of the longitudinal direction by wet etching becomes more than height H (refer to drawing 22 (h)) of the aluminum film usually etched. In the example mentioned above, since height H of the aluminum film is about 150nm, the lateral amount E of etching is set to 150nm or more. Therefore, in order to avoid the problem mentioned above, it is necessary to make distance D between components into twice [more than / more than], i.e., 300nm, the lateral amount E of etching, and it becomes very difficult to perform detailed-ization. Although detailed-ization of extent which is making height H of the aluminum film low is attained, since gate resistance increases by reduction of height H of the aluminum film, it does not become an essential solution.
[0024] Moreover, with the conventional technique mentioned above, a big problem arises also to the dependability of gate dielectric film etc. Hereafter, this problem is explained.
[0025] In the conventional technique mentioned above, in the process of drawing 22 (h), after removing the aluminum film 513 of a P type field by wet etching, the cobalt film 515 is formed in the removed field at drawing 23 (i) and the process of (j). Therefore, by etching of the aluminum film 513 etc., the front face of gate dielectric film 512 will deteriorate, and a bad influence will arise to the dependability of gate dielectric film.

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, it is possible by optimizing the work function of the gate electrode of N type and each P type MIS transistor to optimize the threshold electrical potential difference of N type and a P type MIS transistor. Moreover, it becomes it is possible to attain detailed-izing of a semiconductor device and low resistance-ization, and possible to raise the dependability of a gate electrode etc. further.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As stated above, since etching advanced deeply in a longitudinal direction in case etching removal of the dummy gate is carried out, there was a problem that detailed-izing was difficult, with the conventional DAMASHIN gate technique. Moreover, there was also a problem of having a bad influence on the dependability of gate dielectric film etc., by carrying out etching removal of the dummy gate.
[0027] This invention is made to the above-mentioned conventional problem, sets it as the 1st purpose to attain detailed-ization of a semiconductor device in the semiconductor device with which a gate electrode is produced using a DAMASHIN gate technique etc., and sets it as the 2nd purpose to secure the dependability of a gate electrode etc.

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MEANS

[Means for Solving the Problem] This invention (invention A) is a semiconductor device with which the gate electrode of an N type MIS transistor and each P type MIS transistor is formed through gate dielectric film in the crevice formed in the semi-conductor substrate. One [at least] gate electrode of an N type MIS transistor and a P type MIS transistor is constituted by the laminated structure of two or more metal content film. That and it is smaller than the work function (W2) of the part of the metal content film with which the work function (W1) of the part of the metal content film which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least It considers as the description.
[0029] This invention (invention B) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which removes the 1st metal content film formed in one field of the 1st or 2nd gate formation field, It consists of a process which embeds the crevice of the field of the both sides of the 1st and 2nd gate formation fields by forming the 2nd metal content film on the 1st metal content film saved to the field of another side of the 1st or 2nd gate formation field, and the gate dielectric film of one field of the 1st or 2nd gate formation field. The inside of said 1st and 2nd metal content film, The work function of the part of the metal content film of the direction where the work function (W1) of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least It is characterized by being smaller than (W2).
[0030] This invention (invention C) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which removes the 1st metal content film formed in one field of the 1st or 2nd gate formation field, The process which forms the 3rd metal content film on the 1st metal content film saved to the field of another side of the 1st or 2nd gate formation field, and the gate dielectric film of one field of the 1st or 2nd gate formation field, The process which removes the 3rd metal content film formed in the field of another side of the 1st or 2nd gate formation field, By forming the 2nd metal content film on the 1st metal content film exposed to the field of another side of the 3rd metal content film top saved to one field of the 1st or 2nd gate formation field, and the 1st or 2nd gate formation field It consists of a process which embeds the crevice of the field of the both sides of the 1st and 2nd gate formation fields. The inside of said 1st and 2nd metal content film, The work function of the part of the metal content film of the direction where the work function (W1) of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor whicl touches gate dielectric film at least touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least It is characterized by being smaller than (W2).
[0031] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor is smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this invention (invention A, B, and C), the work function of the gate electrode of N type and each P

type MIS transistor can be optimized, and it is possible to optimize the threshold electrical potential difference of N type and a P type MIS transistor.
[0032] Moreover, according to this invention (invention A, B, and C), since one [at least] gate electrode of an N type MIS transistor and a P type MIS transistor is formed by two or more metal content film, even if its resistivity of the film of the part which touches gate dielectric film is not low, resistance of the whole gate electrode can be made low by preparing the film with low resistivity in an upper layer side.
[0033] Moreover, according to this invention (invention B and C), since the 2nd metal content film is formed on the 1st and 3rd metal content film, thickness of the 1st and 3rd metal content film can be made thin. Therefore, in case the metal content film (the 1st, 3rd metal content film) formed in one field of the 1st or 2nd gate formation field is removed, it can prevent that etching advances deeply to the field of another side of the 1st or 2nd gate formation field, and it becomes possible to attain detailed-ization of a semiconductor device.
[0034] In addition, it is desirable that a work function W1 is in the side near [center / (one half of locations of a band gap) / of the band gap of the semi-conductor used for a semi-conductor substrate] a conduction band in this invention (invention A, B, and C), and a work function W2 is in the side near [center / of a band gap] a load electronic band. Moreover, although the thickness of the field which touches the gate dielectric film which determines the threshold of an MIS transistor should just be more than thickness from which a desired threshold is obtained, it is made to become more than 10 atomic-layer extent preferably.
[0035] Moreover, what is necessary is just to be able to change both work function by changing a presentation or the crystal structure among both in this invention (invention A, B, and C), even if each part which touches the gate dielectric film of N type and a P type MIS transistor does not necessarily need to be an ingredient of a different kind and is an ingredient of the same kind.
[0036] This invention (invention D) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, It consists of a process which changes the 1st metal content film into the 2nd metal content film by making the matter contained in the 1st metal content film formed in one field of the 1st or 2nd gate formation field, and matter other than this matter react. The inside of said 1st and 2nd metal content film, The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.
[0037] This invention (invention E) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, The process which changes the 1st metal content film into the 2nd metal content film by making the matter contained in the 1st metal content film formed in one field of the 1st or 2nd gate formation field, and matter other than this matter react, It consists of a process which changes the 1st metal content film into the 3rd metal content film by making the matter contained in the 1st metal content film formed in the field of another side of the 1st or 2nd gate formation field, and matter other than this matter react. The inside of said 2nd and 3rd metal content film, The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.
[0038] This invention (invention F) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, It consists of a process which forms the 2nd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface. the inside

of the 1st metal content film formed in one field of the 1st or 2nd gate formation field -- this -- among said 1st and 2nd metal content film The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.

[0039] This invention (invention G) is the manufacture approach of the semiconductor device which forms the gate electrode of an N type MIS transistor and each P type MIS transistor through gate dielectric film in the crevice formed in the semi-conductor substrate. The process which forms the 1st metal content film on the gate dielectric film with which the process which forms said gate electrode was formed in the crevice of the field of the both sides of the 1st gate formation field for N type MIS transistors, and the 2nd gate formation field for P type MIS transistors, the inside of the 1st metal content film formed in one field of the 1st or 2nd gate formation field -- this -- with the process which forms the 2nd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface It consists of a process which forms the 3rd metal content film by diffusing matter other than the matter contained in the 1st metal content film, and depositing a gate-dielectric-film interface. the inside of the 1st metal content film formed in the field of another side of the 1st or 2nd gate formation field -- this -- among said 2nd and 3rd metal content film The work function of the part of the metal content film of the direction which touches the gate dielectric film of an N type MIS transistor which touches gate dielectric film at least is characterized by being smaller than the work function of the part of the metal content film of the direction which touches the gate dielectric film of a P type MIS transistor which touches gate dielectric film at least.

[0040] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor is smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this invention (invention D, E, F, and G), the work function of the gate electrode of N type and each P type MIS transistor can be optimized, and it is possible to optimize the threshold electrical potential difference of N type and a P type MIS transistor.

[0041] Moreover, change the 1st metal content film into the 2nd and 3rd metal content film by making the matter contained in the 1st metal content film, and matter other than this matter react according to this invention (invention D, E, F, and G). Or since the 2nd and 3rd metal content film is formed by diffusing matter other than the matter contained in the 1st metal content film in the inside of the 1st metal content film, and depositing a gate-dielectric-film interface A gate electrode can be produced without etching the metal content film formed on the gate dielectric film in a crevice, and it is possible to prevent the fall of the dependability of gate dielectric film.

[0042] In addition, it is desirable that a work function W1 is in the side near [center / (one half of locations of a band gap) / of the band gap of the semi-conductor used for a semi-conductor substrate] a conduction band in this invention (invention D, E, F, and G), and a work function W2 is in the side near [center / of a band gap] a load electronic band. Moreover, although the thickness of the field which touches the gate dielectric film which determines the threshold of an MIS transistor should just be more than thickness from which a desired threshold is obtained, it is made to become more than 10 atomic-layer extent preferably.

[0043]

[Embodiment of the Invention] Hereafter, the operation gestalt of this invention is explained with reference to a drawing.

[0044] (Operation gestalt 1) An example of the production process concerning the 1st operation gestalt of this invention is hereafter explained with reference to drawing 1 (a) - drawing 3 (i).

[0045] First, the isolation 102 of STI structure is formed on a silicon substrate 101. Then, silicon oxide 103 of about 2-6nm of thickness is formed as a dummy insulator layer removed in the future. Furthermore, the laminated structure of the polish recon film 104 of about 150nm of thickness and the silicon nitride 105 of about 50nm of thickness is formed as the dummy gate removed in the future. These dummy insulator layers and the dummy gate are formed using the usual techniques (membrane formation techniques, such as oxidation and CVD, a lithography technique, RIE technique, etc.). Then, the impurity diffused layer for extensions used as the source drain diffusion layer 106 is formed with an ion-implantation technique by using the dummy gate (the polish recon film 104 and silicon nitride 105) as a mask. Then, a gate side-attachment-wall insulator layer with a width of face of about 20-40nm which consists of a silicon nitride 107 is formed with a CVD technique and a RIE technique (drawing 1 (a)).

[0046] Next, the high concentration impurity diffused layer used as the source drain diffusion layer 108 is formed

with an ion-implantation technique by using the dummy gate (the polish recon film 104 and silicon nitride 105) and a gate side-attachment-wall insulator layer (silicon nitriding 107) as a mask. Furthermore, the silicide film (silicide, such as cobalt or titanium) 109 with a thickness of about 40nm is formed only in a source drain field by using the dummy gate as a mask with a salicide process technique (drawing 1 (b)).
[0047] Next, silicon oxide is deposited with a CVD method as an interlayer insulation film 110. Furthermore, the front face of the silicon nitrides 105 and 107 is exposed by carrying out flattening of this interlayer insulation film 110 with a CMP technique (drawing 1 (c)).
[0048] Next, the silicon nitride 105 of the dummy gate upper part is alternatively removed to an interlayer insulation film 110, for example using phosphoric acid. At this time, the silicon nitride 107 is also etched to height extent of the polish recon film 104. Then, the etching technique using the radical of halogen atoms, such as a fluorine, removes the polish recon film 104 alternatively to an interlayer insulation film 110 and the silicon nitride 107, for example (drawing 2 (d)).
[0049] Next, a slot (crevice) 111 is formed by removing dummy silicon oxide 103 by wet etching, such as rare fluoric acid. Then, the hafnium oxide film (HfO2 film) which is a high dielectric insulator layer is formed in the whole surface as gate dielectric film. This hafnium oxide film is HfCl4. NH3 It is obtained by oxidizing the hafnium nitride which formed membranes by the spatter using the target of the used CVD method, a hafnium nitride (HfN), or a hafnium, after forming a hafnium nitride (HfN film) (drawing 2 (e)).
[0050] Next, the hafnium nitride 113 whose work function is about 4eV is desirably formed on the whole surface by 10nm or less about 10nm in thickness using a CVD method or a spatter (drawing 2 (f)).
[0051] Although the process of the above drawing 1 (a) - drawing 2 (f) was performed to the both sides of an N type MIS transistor formation field and a P type MIS transistor formation field, it showed only one field on the drawing. From future processes, the both sides of an N type MIS transistor (N type MISFET) formation field and a P type MIS transistor (P type MISFET) formation field are shown on a drawing.
[0052] It covers except a P type MIS transistor formation field by the resist 114 after the process of drawing 2 (f) using a lithography technique. The top view of the principal part at this time is typically shown in drawing 4 (a) (drawing 3 (g)).
[0053] Next, only a P type field removes the hafnium nitride 113 by performing wet etching by hydrogen peroxide solution. The top view of the principal part at this time is typically shown in drawing 4 (b). Since the hafnium oxide film 112 of gate dielectric film is insoluble to hydrogen peroxide solution, it is not etched. Moreover, since the hafnium nitride 113 is very thin (about 10nm), unlike the case of the conventional technique, the hafnium nitride 113 is not deeply etched to an N type field. that is, in this example, the thickness of the hafnium nitride 113 is about 10nm -- it comes out and the lateral amount E of etching is set to about 10nm. Therefore, if the distance D between components is about 20nm or more, the trouble of the conventional technique can be canceled and it will become possible to perform large detailed-ization (drawing 3 (h)).
[0054] Next, after removing resist 114, a work function deposits the cobalt film 115 on the whole surface as noble-metals film which is about 5eV. Membrane formation of cobalt is performed using a spatter, or they are Co (CO)4 and Co2. 8, CoF2, and CoCl2 Or CoBr2 It carries out using the CVD method used as the gas source. Then, with a CMP technique, flattening of the cobalt film 115, the hafnium nitride 113, and the hafnium oxide film 112 is performed until an interlayer insulation film 110 is exposed. The top view of the principal part at this time is typically shown in drawing 4 R> 4 (c) (drawing 3 (i)).
[0055] According to the above process, as gate electrode structure, N type consists of a laminated structure of the hafnium nitride 113 and the cobalt film 115, and C-MIS transistor which consists of monolayer structure of the cobalt film 115 completes P type.
[0056] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor can be made smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this operation gestalt (a work function is [the hafnium nitride 113 / a work function] about 5eV at the example mentioned above for about 4eV and the cobalt film 115), it is possible to optimize the work function of the gate electrode of N type and each P type MIS transistor, and to optimize the threshold electrical potential difference of both transistors.
[0057] Moreover, with this operation gestalt, in case the hafnium nitride 113 of a P type field is removed, since the thickness of the hafnium nitride 113 is very thin, it can avoid that the hafnium nitride 113 is deeply etched to an N type field, and it becomes possible to perform large detailed-ization. Furthermore, with this operation gestalt, since the cobalt film 115 of low resistance is formed on the hafnium nitride 113, the gate electrode of an N type MIS transistor can reconcile optimization of a work function, and low resistance-ization.

[0058] Drawing 5 shows the component separation distance (distance between components, distance D shown in drawing 4) dependency of a threshold (threshold voltage) about the N type and the P type MIS transistor by this operation gestalt and the conventional technique.
[0059] In this operation gestalt and the conventional technique, about the P type MIS transistor, the threshold serves as [the component separation distance D] regularity and a low battery (about -0.2V) to about 400nm. On the other hand, about an N type MIS transistor, a threshold is beginning to rise [the distance D between components] by 300nm or less with the conventional technique. This is because it consists of metals a part of whose N type MIS transistors are about 5.0eV of work functions. On the other hand, with this operation gestalt, even if it makes distance D between components detailed to 40nm, it turns out that a threshold is fixed.
[0060] In the example mentioned above, the gate electrode of an N type MIS transistor explained the case where the gate electrode of a P type MIS transistor was the monolayer structure of the cobalt film, by the laminated structure of a hafnium nitride and the cobalt film. Not only gate electrode structure such but various deformation is possible for this operation gestalt. Then, some modifications are explained below.
[0061] the fundamental gate structure in this operation gestalt -- three kinds, Structure A, Structure B, and Structure C, -- it is . About Structure A, drawing 7 corresponds about Structure B and drawing 8 corresponds [drawing 6 / Structure / C], respectively. About such structures A, Structure B, and Structure C, structure (it considers as Structure D) as shown in drawing 9 is also included as a variation of such structures. In addition, drawing 6 - drawing 9 show only gate dielectric film and a gate electrode typically.
[0062] The gate electrode of an N type MIS transistor consists of the 1st metal content film F1 and the 2nd metal content film F2 which were formed on gate dielectric film F0, the gate electrode of a P type MIS transistor consists of the 2nd metal content film F2 formed on gate dielectric film F0, and Structure A (refer to drawing 6) has the work function of the 1st metal content film F1 smaller than the work function of the 2nd metal content film F2.
[0063] The process at which the manufacture approach of Structure A forms the 1st metal content film F1 on the gate dielectric film F0 of the gate formation field of the both sides for N type and P type MIS transistors, The process which removes the 1st metal content film F1 of the gate formation field for P type MIS transistors, By forming the 2nd metal content film F2 on the 1st [of the gate formation field for N type MIS transistors] metal content film F1, and the gate dielectric film F0 of the gate formation field for P type MIS transistors It consists of a process which embeds the crevice of the gate formation field of the both sides of N type and a P type MIS transistor.
[0064] The gate electrode of a P type MIS transistor consists of the 1st metal content film F1 and the 2nd metal content film F2 which were formed on gate dielectric film F0, the gate electrode of an N type MIS transistor consists of the 2nd metal content film F2 formed on gate dielectric film F0, and the work function of structure of the 1st metal content film F1 is [B (refer to drawing 7)] smaller than the work function of the 2nd metal content film F2.
[0065] The process at which the manufacture approach of Structure B forms the 1st metal content film F1 on the gate dielectric film F0 of the gate formation field of the both sides for N type and P type MIS transistors, The process which removes the 1st metal content film F1 of the gate formation field for N type MIS transistors, By forming the 2nd metal content film F2 on the 1st [of the gate formation field for P type MIS transistors] metal content film F1, and the gate dielectric film F0 of the gate formation field for N type MIS transistors It consists of a process which embeds the crevice of the gate formation field of the both sides of N type and a P type MIS transistor.
[0066] It is as drawing 1 - drawing 3 R> 3 having shown the concrete example of Structure A. Moreover, about Structure B, most manufacture approaches shown in drawing 1 - drawing 3 can be diverted (the thing suitable for Structure B is used for each component). Main changed parts are points which carry out the mask of the P type MIS transistor field by the resist instead of an N type MIS transistor field in the process of drawing 3 (g).
[0067] Structure C (refer to drawing 8) consists of the 1st metal content film F1 and the 2nd metal content film F2 with which the gate electrode of an N type MIS transistor was formed on gate dielectric film F0. The gate electrode of a P type MIS transistor consists of the 3rd metal content film F3 and the 2nd metal content film F2 which were formed on gate dielectric film F0, and the work function of the 1st metal content film F1 is smaller than the work function of the 3rd metal content film F3.
[0068] The process at which the manufacture approach of Structure C forms the 1st metal content film F1 on the gate dielectric film F0 of the gate formation field of the both sides for (refer to drawing 10), N type, and P type MIS transistors, The process which removes the 1st metal content film F1 of the gate formation field for P

type MIS transistors, The process which forms the 3rd metal content film F3 on the 1st [of the gate formation field for N type MIS transistors] metal content film F1, and the gate dielectric film F0 of the gate formation field for P type MIS transistors, The process which removes the 3rd metal content film F3 of the gate formation field for N type MIS transistors, By forming the 2nd metal content film F2 on the 1st [of the gate formation field for N type MIS transistors] metal content film F1, and the 3rd [of the gate formation field for P type MIS transistors] metal content film F3 It consists of a process which embeds the crevice of the gate formation field of the both sides of N type and a P type MIS transistor.

[0069] In addition, the structure (structure D) where the 2nd metal content film F2 is two or more kinds of cascade screens is also included in Structure A, Structure B, and Structure C. Corresponding to the example of drawing 6 , the 2nd metal content film F2 of N type and a P type MIS transistor is constituted from an example of drawing 9 by the cascade screen of metal content film F2a and F2b.

[0070] Hereafter, the structure A mentioned above - Structure D are explained further.

[0071] (1) In Structure A (refer to drawing 6), the 2nd metal content film F2 is used as a barrier metal which determines the threshold of a P type MIS transistor, respectively as a barrier metal the 1st metal content film F1 decides the threshold of an N type MIS transistor to be.

[0072] What has possible performing etching (wet etching or dry etching by the radical atom or the radical molecule) which has the work function (4.6eV or less, desirably about 4eV) which can optimize the threshold of an N type MIS transistor, and does not have a damage is used for the 1st metal content film F1. HfN and ZrN are raised to a typical ingredient. These are expected that a work function is about 4eV, and are suitable as a barrier metal of N type.

[0073] What has the low resistivity which has the work function (4.6eV or more, desirably about 5eV) which can optimize the threshold of a P type MIS transistor, and can carry out [low ****]-izing of the gate electrode is used for the 2nd metal content film F2. The ingredient of a noble-metals system has many whose work function is about 5eV, and fits the 2nd metal content film. For Co, from a viewpoint of resistivity, about 5micro ohm-cm and nickel are [about 6micro ohm-cm and Pt] about 10micro ohm-cm. W and CoSi2 which are used as a current gate electrode Resistivity is about 5micro ohm-cm and about 20micro ohm-cm, respectively, and Co, nickel and Pt, especially Co are suitable as an ingredient of the 2nd metal content film.

[0074] It is HfO2 when barrier metal is HfN, although not limited especially about gate dielectric film F0. Using is desirable. HfN and HfO2 It is because thermal reaction cannot occur easily in an interface.

[0075] (2) In Structure B (refer to drawing 7), the 2nd metal content film F2 is used as a barrier metal which determines the threshold of an N type MIS transistor, respectively as a barrier metal the 1st metal content film F1 decides the threshold of a P type MIS transistor to be.

[0076] What has possible performing etching (wet etching or dry etching by the radical atom or the radical molecule) which has the work function (4.6eV or more, desirably about 5eV) which can optimize the threshold of a P type MIS transistor, and does not have a damage is used for the 1st metal content film F1. In a typical ingredient, it is WNx. And WSix Ny It is raised.

[0077] What has the low resistivity which has the work function (4.6eV or less, desirably about 4eV) which can optimize the threshold of an N type MIS transistor, and can carry out [low ****]-izing of the gate electrode is used for the 2nd metal content film F2. aluminum (or alloy containing aluminum) is raised as a typical ingredient.

[0078] (3) In Structure C (refer to drawing 8), as a barrier metal the 1st metal content film F1 decides the threshold of an N type MIS transistor to be, the 3rd metal content film F3 is used as a barrier metal which determines the threshold of a P type MIS transistor, respectively, and the 2nd metal content film F2 is used as an electrode material of low resistance.

[0079] what has possible performing etching (wet etching or dry etching by the radical atom or the radical molecule) which has the work function (4.6eV or less, desirably about 4eV) which can optimize the threshold of an N type MIS transistor on the 1st metal content film F1, and does not have a damage in it -- HfN is used typically. what has possible performing etching which has the work function (4.6eV or more, desirably about 5eV) which can optimize the threshold of a P type MIS transistor on the 3rd metal content film F3, and does not have a damage in it -- typical -- WNx It uses. aluminum (or alloy containing aluminum) is used for the 2nd metal content film F2 at the ingredient and representation target which are low resistance.

[0080] (4) With the structure A in Structure D (refer to drawing 9), or the structure corresponding to Structure B As 2nd metal content film F2 which is a cascade screen, it is the work function (about N type, 4.6eV or less) which can optimize the threshold of N type or a P type MIS transistor about film F2a by the side of a lower layer. About 4eV and P type, it is called for desirably that it is [4.6eV or more] low resistance to have 5eV desirably

at film F2b by the side of the upper layer.
[0081] With the structure corresponding to the structure C in Structure D, although there is no merit of using the film by the side of the lower layer of the 2nd metal content film in order to optimize the threshold of a transistor since the 1st metal content film F1 and the 3rd metal content film F3 are under the 2nd metal content film F2, there is a merit that diffusion of the metal to the gate dielectric film from an upper layer side can be controlled.
[0082] Typically, it structure D Sets and the thing corresponding to Structure A which constituted [the 1st metal content film F1] upper layer side F2b of RuO2 and the 2nd metal content film for lower layer side F2a of HfN and the 2nd metal content film from aluminum is raised.
[0083] (5) In Structure A, Structure B, and Structure C, it is desirable to use for the 1st metal content film F1 the metallic compounds which are conductors. As a barrier metal for N type MIS transistors, a hafnium nitride, a zirconium nitride, a titanium nitride, a tantalum nitride, a tantalum nitride, and a niobium nitride are raised. A tungsten nitride and a tungsten silicification nitride are raised as a barrier metal for P type MIS transistors.
[0084] (6) In Structure A and Structure C, it is desirable to use the film which contains the alloy containing platinum, palladium, nickel, cobalt, a rhodium, a ruthenium, a rhenium, iridium, gold, silver, copper, or these metals in the 2nd metal content film F2.
[0085] (7) In Structure A, Structure B, and Structure C, it is desirable to use for the 2nd metal content film F2 the film containing the metallic compounds which are conductors.
[0086] As metallic compounds, a metallic oxide (ruthenium oxide, an iridium acid ghost, rhenium oxide, platinum oxide, rhodium oxide) is raised [1st]. Noble-metals system oxide is a conductor in many cases, and is for being easy to obtain the work function suitable for a P type MIS transistor.
[0087] As metallic compounds, metal silicide (platinum silicide, palladium silicide, nickel silicide) is raised to the 2nd. These can obtain the work function suitable for N type or a P type MIS transistor (especially P type MIS transistor).
[0088] As metallic compounds, a metal nitride (a hafnium nitride, a zirconium nitride, a titanium nitride, a tantalum nitride, niobium nitride) is raised to the 3rd. These can obtain the work function suitable for an N type MIS transistor.
[0089] (8) In Structure D, it is desirable for the film of the lowest layer to be [of the 2nd metal content film F2] metallic compounds at least. As metallic compounds, a metallic oxide (ruthenium oxide, an iridium acid ghost, rhenium oxide, platinum oxide, rhodium oxide), metal silicide (platinum silicide, palladium silicide, nickel silicide), a metal nitride (a hafnium nitride, a zirconium nitride, a titanium nitride, a tantalum nitride, a niobium nitride, a tungsten nitride, tungsten nitride), and tungsten nitriding silicide are raised.
[0090] (9) In Structure C, it is desirable to use a tungsten nitride or tungsten nitriding silicide for the 3rd metal content film F3.
[0091] In Structure A - Structure D (10) As gate dielectric film F0 HfO2, ZrO2, TiO2, a silicon nitride, and aluminum 2O3, The zirconic acid-ized film containing Ta 2O5, Nb 2O5, Y2 O3, CeO2, and an yttrium, the compound film of barium, strontium, titanium, and oxygen, the compound film of lead, a zirconium, titanium, and oxygen, and silicon oxide are raised.
[0092] By the method of forming the zirconic acid-ized film containing HfO2, ZrO2, TiO2, Ta 2O5, Nb 2O5, Y2 O3, CeO2, and an yttrium It is HfCl4, ZrCl4, TiCl4, TaCl5, NbCl5, and Y(Thd) 3 (here, Thd is 2, 2, 6, and 6-tetramethyl - 3 and 5-hepta-screw ONETO is meant.), respectively. Ce (Thd)4 and Zr4 (Thd) Y(Thd) 3 To mixed gas, it is O2. There is the approach of forming membranes directly with the CVD method which mixed gas.
[0093] O2 [moreover,] instead of [of gas] -- for example, NH3 etc. -- it uses, the zirconium nitride which contains each metal nitride, i.e., HfN, ZrN, TiN, TaN, NbN, YN, and CeN, and an yttrium first is formed, and it may be made to use each metal nitride by thermal oxidation as an oxide after that. When using this thermal oxidation approach, it is desirable to oxidize thermally a nitride 5nm or less, or to make it repeat nitride deposition / oxidation of 5nm or less two or more times so that nitrogen may not remain in the film. When a thick nitride is oxidized thermally and oxidation temperature is low temperature 500 degrees C or less, it is because it was founc out that it becomes impossible for the nitrogen which is a product from the layer which newly oxidized to escape from the interior of membranous outside, and it remains in the film.
[0094] Moreover, before forming the metallic oxide mentioned above, the gate dielectric film F0 of a laminated structure may be produced by forming the silicon nitride by the oxidation nitride using oxidation in the silicon oxide by thermal oxidation, and NO gas etc., or the CVD method on a silicon substrate, and forming the metal oxide film mentioned above after that.
[0095] (11) As film by the side of the lowest layer of a gate electrode, when using HfN, ZrN, and TiN, hydrogen

peroxide solution can be used for these etching. It is required not to etch gate dielectric film F0 at the time of etching using this hydrogen peroxide solution. HfO2 mentioned above as gate dielectric film F0, ZrO2, TiO2, and Si3 N4, aluminum 2O3, Ta 2O5, Nb 2O5, and Y2 O3, Since these are insoluble to hydrogen peroxide solution when using the zirconic acid-ized film containing CeO2 and an yttrium, the compound film of barium, strontium, titanium, and oxygen, the compound film of lead, a zirconium, titanium, and oxygen, and silicon oxide, a problem is not produced.

[0096] As film by the side of the lowest layer of a gate electrode, when using TaN and NbN, these are meltable into the mixed liquor of a hydrochloric acid and a nitric acid. Therefore, what is necessary is just to use for gate dielectric film F0 silicon oxy-night RAIDO which contains insoluble HfO2, ZrO2, TiO2, Si3 N4, silicon oxide, and nitrogen 1% or more into this mixed liquor.

[0097] When using aluminum as film by the side of the lowest layer of a gate electrode, aluminum is meltable into the mixed liquor of phosphoric acid and a nitric acid. Therefore, what is necessary is just to use the zirconic acid-ized film which contains insoluble HfO2, ZrO2, TiO2, Ta 2O5, Nb 2O5, and an yttrium in gate dielectric film F0 at this mixed liquor, the compound film of barium, strontium, titanium, and oxygen, the compound film of lead, a zirconium, titanium, and oxygen, and silicon oxide.

[0098] (12) When the metal nitride (HfN, ZrN, TiN, TaN, NbN) mentioned above as film by the side of the lowest layer of a gate electrode is used, as for how of the metal nitride film and gate dielectric film to combine, it is desirable to fulfill the following conditions other than the etching resistance mentioned above. That is, it is made for the free energy of Gibbs of the metallic oxide which consists of a metallic element which constitutes a metal nitride to become below the free energy of Gibbs of the metal oxide film used for gate dielectric film, or silicon oxide. When it does in this way, it is for possibility that a metal nitride will return gate dielectric film to decrease. Specifically, gate dielectric film is HfO2. It is desirable to use HfN, ZrN, TiN, TaN, and NbN for a case as a metal nitride, and gate dielectric film is Ta 2O5. It is desirable to use TaN and NbN for a case as a metal nitride.

[0099] (Operation gestalt 2) An example of the production process concerning the 2nd operation gestalt of this invention is hereafter explained with reference to drawing 11 (a) - Fig. 1414 (l).

[0100] First, the front face of a silicon substrate 201 is oxidized thermally, and silicon oxide 202 is formed. Then, the silicon nitride 203 is formed on silicon oxide 202 using a CVD method (drawing 11 (a)).

[0101] Next, the pattern of a photoresist 204 is formed on the silicon nitride 203. Then, an isolation slot is formed by using this resist pattern 204 as a mask, and carrying out patterning of the silicon nitride 203, silicon oxide 202, and the silicon substrate 201 using anisotropic etching (drawing 11 (b)).

[0102] Next, a photoresist 204 is ashed and removed. Then, it is the front face of the exposed isolation slot 950 degrees C and HCl/O2 Silicon oxide 205 is formed by oxidizing thermally in an ambient atmosphere. Then, silicon oxide 206 is deposited on the whole surface using a CVD method, and an isolation slot is embedded. Furthermore, it grinds until the front face of the silicon nitride 203 exposes silicon oxide 206 using the CMP method (drawing 11 (c)).

[0103] Next, the silicon nitride 203 is alternatively removed using heat phosphoric acid. Then, silicon oxide 202 is removed using a rare fluoric acid solution. In this case, the upside silicon oxide 206 and the silicon oxide 205 of an isolation slot are etched somewhat, and the front face of the silicon substrate 201 near the up edge of an isolation slot is exposed (drawing 12 (d)).

[0104] Next, 900 degrees C and HCl/O2 It oxidizes thermally in an ambient atmosphere and the silicon oxide 207 used as a dummy insulator layer is formed. Since the dummy insulator layer 207 is formed not only an MIS transistor formation field top but on the up edge of an isolation slot, the exposure of a silicon substrate of it is lost (drawing 12 (e)).

[0105] Next, after forming the polish recon film 208 in the whole surface, the dummy gate is formed by carrying out patterning of this polish recon film 208 (drawing 12 (f)).

[0106] Next, the dummy gate which consists of polish recon film 208 is used as a mask, and impurity ion is injected into the front face of a silicon substrate 201. Furthermore, the source drain diffusion layer 209 is formed in self align to the dummy gate by performing hot annealing treatment. Then, an interlayer insulation film 210 is deposited on the whole surface, and flattening is carried out until the polish recon film 208 exposes this interlayer insulation film 210 using the CMP method. Then, it is the exposed polish recon film 208 CF4 / O2 The downflow technique using gas removes (drawing 13 (g)).

[0107] Next, in order to adjust the threshold electrical potential difference of N type and each P type MIS transistor, the impurity of N type and P type is introduced with ion-implantation into a silicon substrate 201 through the exposed dummy insulator layer 207, respectively. Then, a slot (crevice) 211 is formed by removing

the dummy insulator layer 207 using a rare fluoric acid solution. Then, it is Ta 2O5 as gate dielectric film. The film 212 is formed. Furthermore, the ruthenium (Ru) film or the palladium (Pd) film 213 is formed about 10nm of thickness as a gate electrode material of a P type MIS transistor (drawing 13 R> 3 (h)).

[0108] Next, the silicon nitride 214 is formed in the whole surface by 10nm thickness by the plasma-CVD method. This silicon nitride 214 is used as diffusion prevention film for preventing diffusion of the indium (In) or tin (Sn) formed at a next process. Then, the pattern of a photoresist 215 is formed on a P type MIS transistor field (drawing 13 (i)).

[0109] Next, the silicon nitride 214 of the exposed N type MIS transistor field is removed using the downflow method. a photoresist 215 -- ashing -- after processing removes, the indium (In) film or the tin (Sn) film is formed in the whole surface by 1-2nm thickness as a gate electrode material of an N type MIS transistor (drawing 14 (j)).

[0110] Next, inside [of 200 degrees C - about 400 degrees C] low-temperature annealing is performed. Since the silicon nitride 214 is formed in the P type MIS transistor field, an indium or tin is alternatively spread only to an N type MIS transistor field by this annealing treatment. An indium or tin is diffused through the grain boundary of the ruthenium film or the palladium film 213. Ta 2O5 from which an indium or tin serves as gate dielectric film by this It deposits in an interface with the film 212, the ruthenium film, or the palladium film 213. Consequently, the indium film or the tin film 216 used as the gate electrode of an N type MIS transistor is formed (drawing 14 (k)).

[0111] Next, the indium film or the tin film 216 on a P type MIS transistor field is removed alternatively, and the silicon nitride 214 is further removed using the downflow method. Then, the tungsten film 217 is embedded in the slot of the gate electrode field of N type and a P type MIS transistor. furthermore, the CMP method -- using -- the ruthenium film outside a slot or the palladium film 213, the indium film or the tin film 216, and Ta 2O5 The film 212 and the tungsten film 217 are removed, and it leaves only Mizouchi the tungsten film 217. Thereby, the gate electrode with which the indium film or the tin film 216 was formed in the lowest layer for the gate electrode with which the ruthenium film or the palladium film 213 was formed in the lowest layer with the N type MIS transistor consists of P type MIS transistors. Henceforth, an interlayer insulation film 218 and wiring 219 grade are formed, and a semiconductor integrated circuit is completed (drawing 14 (l)).

[0112] In addition, the metal M1 (in the example mentioned above) which constitutes the gate electrode of a P type MIS transistor from an example mentioned above Although it was made to deposit a metal M2 in the gate-dielectric-film interface of an N type MIS transistor by diffusing the metal M2 (the example mentioned above an indium or tin) which constitutes the gate electrode of an N type MIS transistor for the inside of a ruthenium or palladium The alloy of a metal M1 and a metal M2 is formed, and you may make it this alloy constitute the gate electrode of an N type MIS transistor by diffusing a metal M2 in a metal M1 (it considers as a modification 1).

[0113] Moreover, in case the metal M2 which constitutes the gate electrode of an N type MIS transistor for the inside of the metal M1 which constitutes the gate electrode of a P type MIS transistor from an example mentioned above is diffused Although it was made to make an N type MIS transistor field diffuse a metal M2 alternatively by using as a mask of diffusion of the silicon nitride 214 The silicon nitride 214 forms a metal M2 alternatively only on the metal M1 of an N type MIS transistor field, and you may make it diffuse a metal M2 in a metal M1 alternatively only in an N type MIS transistor field like the example mentioned above, without forming (it considers as a modification 2).

[0114] Furthermore, although the basic example and modifications 1 and 2 which were mentioned above deposit a metal M2 in a gate-dielectric-film interface or are performing the approach of forming the alloy of a metal M1 and a metal M2, to the gate electrode of an N type MIS transistor, they may perform the same approach to the gate electrode of a P type MIS transistor.

[0115] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor can be made smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this operation gestalt, it is possible to optimize the work function of the gate electrode of N type and each P type MIS transistor, and to optimize the threshold electrical potential difference of both transistors. Moreover, since etching removal of the metal membrane formed in Mizouchi for gate electrode formation is not carried out like before with this operation gestalt, it is possible to control the fall of the dependability of gate dielectric film.

[0116] (Operation gestalt 3) An example of the production process is hereafter explained with reference to drawing 1515 (a) - drawing 17 (h) about the 1st example concerning the 3rd operation gestalt of this invention.

[0117] first, a silicon substrate 301 top -- isolation 302 -- forming -- then, an N type MIS transistor field -- the

well of P type -- a diffusion layer 303 -- a P type MIS transistor field -- the well of N type -- a diffusion layer 304 is formed (drawing 15 (a))
Next, about 5nm oxidizes the front face of the exposed silicon substrate 301, and the silicon oxide 305 used as a dummy insulator layer is formed. Then, the polish recon film 306 used as the dummy gate is deposited, and patterning of this is carried out to the configuration of a gate electrode. Then, the poly SHIRIKO film 306 used as the dummy gate is used as a mask, arsenic is made an N type field, the ion implantation of the boron is made to a P type field, and the shallow impurity diffused layer used as the source drain diffusion layer 307 is formed. Then, the silicon nitride 308 is deposited and a side-attachment-wall insulator layer is formed by carrying out anisotropic etching of this. Then, this side-attachment-wall insulator layer 308 and the polish recon film 306 are used as a mask, arsenic is made an N type field, the ion implantation of the boron is made to a P type field, and the deep impurity diffused layer used as the source drain diffusion layer 309 is formed (drawing 15 (b)).
[0118] Next, silicon oxide is deposited on the whole surface as an interlayer insulation film 310. Then, using the CMP method, flattening is carried out until the polish recon film 306 exposes silicon oxide 310 (drawing 15 (c)).
[0119] Next, the polish recon film 306 is removed using isotropic etching techniques, such as chemical dry etching. Then, etching removal of the exposed silicon oxide 305 is carried out by rare hydrofluoric acid treatment etc., and the slot 311 for gate electrode formation is formed in the both sides of N type and a P type MIS transistor field (drawing 16 (d)).
[0120] Next, the silicon substrate 301 of slot 311 pars basilaris ossis occipitalis for gate electrode formation is oxidized by thermal oxidation processing, and the gate dielectric film which consists of silicon oxide 312 is formed. Then, the tungsten silicide (WSi2) film 313 is deposited on the whole surface with a CVD method as a gate electrode material of an N type MIS transistor. Then, the tungsten silicide film 313 deposited on the exterior of the slot 311 for gate electrode formation by the CMP method is removed, and the tungsten silicide film 313 is made to save only in the slot 311 for gate electrode formation (drawing 16 (e)).
[0121] Next, the silicon nitride 314 is deposited on the whole surface, and only an N type MIS transistor field is made to save the silicon nitride 15 with photolithography and an etching technique further. Then, the palladium (Pd) film 315 is deposited on the whole surface by a spatter etc. (drawing 16 (f)).
[0122] Next, 600 degrees C and 1-minute room [about] annealing treatment are performed. Thereby, the tungsten silicide film 313 currently embedded at the gate electrode section of a P type MIS transistor field reacts with the palladium film 315. Consequently, the palladium silicide (Pd2 Si) film 316 is formed in the field to which the tungsten silicide film 313 existed from the first, and a tungsten is discharged in the palladium film of the upper part of this palladium silicide film 316. In an N type MIS transistor field, since it is formed silicon nitride 314, the tungsten silicide film 313 is not permuted by the palladium silicide film 316. Then, CMP etc. removes the metal and the silicon nitride 314 which remained in the exterior of the slot for gate electrode formation. Thereby, the gate electrode of a P type MIS transistor is formed with the palladium silicide film 316 (drawing 17 (g)).
[0123] Next, the silicon oxide used as an interlayer insulation film 317 is deposited on the whole surface. Then, the hole for the contact which reaches the source drain and gate electrode of an MIS transistor is formed in interlayer insulation films 317 and 310. Then, the metal membrane for wiring 318 is deposited and the MIS transistor transistor of N type and P type is completed by carrying out patterning of this (drawing 17 (h)).
[0124] In addition, although the tungsten silicide (WSi2) film was used as a gate electrode material of an N type MIS transistor in the example mentioned above, it is also possible to use silicide, such as molybdenum silicide (MoSi2), tantalum silicide (TaSi2), niobium silicide (NbSi2), or chromium silicide (CrSi2), instead of tungsten silicide.
[0125] Moreover, by forming the palladium (Pd) film on the tungsten silicide film of a P type MIS transistor field, and making palladium react with the tungsten silicide film by heat treatment in the example mentioned above Although tungsten silicide was permuted by palladium silicide (Pd2 Si, PdSi) It is also possible to use nickel (nickel) or platinum (Pt) instead of palladium, and to permute by silicide, such as nickel silicide (NiSi and NiSi2) or platinum silicide (Pt2 Si, PtSi).
[0126] Moreover, Ta 2O5 formed with the CVD method etc. although the silicon oxide obtained by heat treatment as gate dielectric film was used in the example (even the following examples [2nd and 3rd] are the same) mentioned above You may make it use the film.
[0127] Next, an example of the production process is explained with reference to drawing 18 (a) - Fig. 1818 (c) about the 2nd example concerning the 3rd operation gestalt of this invention.
[0128] In addition, since it is the same as that of the 1st example which the intermediate process (process of drawing 15 (a) - drawing 16 (e)) mentioned above, this example explains the process after the process of drawing

16 (e).
[0129] After the process of drawing 16 (e), after carrying out the mask of the N type MIS transistor field by the resist 321, with ion-implantation, the ion implantation of the germanium ion (germanium+) is alternatively carried out only to the tungsten silicide film 313 of a P type MIS transistor field, and it is referred to as tungsten silicide film 313a containing germanium. At this time, concentration of the germanium ion introduced into the tungsten silicide film 313 is made into the concentration more than the solid-solution limit of the germanium in tungsten silicide (about [for example, / 1x1017cm -] 3) (drawing 18 (a)).
[0130] Next, the mask of the P type MIS transistor field is carried out by the resist 322, and with ion-implantation, the ion implantation of the indium ion (In+) is alternatively carried out only to the tungsten silicide film 313 of an N type MIS transistor field, and it is referred to as tungsten silicide film 313b containing an indium. At this time, concentration of the indium ion introduced into the tungsten silicide film 313 is made into the concentration more than the solid-solution limit of the indium in tungsten silicide (about [for example, / 1x1017cm -] 3) (drawing 18 (b)).
[0131] Next, the germanium and the indium which were poured in into the tungsten silicide film 313 deposit in the interface of the tungsten silicide film 313 and the silicon oxide 312 which is gate dielectric film by performing 800 degrees C and heat treatment for about 1 minute. Consequently, in a P type MIS transistor, a gate electrode is formed of the laminated structure of the germanium film 323 and the tungsten silicide film 313, and a gate electrode is formed in an N type MIS transistor of the laminated structure of the indium film 324 and the tungsten silicide film 313 (drawing 18 (c)).
[0132] Finally, the MIS transistor of N type and P type is completed like the 1st example by depositing an interlayer insulation film, making the hole for contact, and forming wiring further.
[0133] In addition, although the tungsten silicide (WSi2) film was used in the example mentioned above as an ingredient beforehand formed into the slot for gate electrodes, it is also possible to use molybdenum silicide (MoSi2), tantalum silicide (TaSi2), niobium silicide (NbSi2), or chromium silicide (CrSi2) instead of tungsten silicide.
[0134] Moreover, although the indium (In) was used with germanium (germanium) and an N type MIS transistor with the P type MIS transistor, a suitable ingredient is chosen out of germanium, an indium, antimony (Sb), platinum (Pt), palladium (Pd), etc., and you may make it deposit a separate ingredient with both the transistors of P type and N type in the example mentioned above as an ingredient which deposits a gate-dielectric-film interface. Moreover, these ingredients are deposited only about one transistor of P type or N type (it is a deed about an ion implantation only about one transistor), and you may make it use a gate electrode material (the example mentioned above tungsten silicide) from the first as a gate electrode as it is with the transistor of another side.
[0135] Furthermore, although it was made to deposit the matter which carried out the ion implantation in a gate-dielectric-film interface by heat treatment in the example mentioned above, the reactant of each matter which carried out the ion implantation of the separate matter to the gate electrode field of P type and an N type MIS transistor, and carried out the ion implantation by heat treatment etc., and the gate electrode material currently formed in the gate electrode field from the first is formed, and you may make it the work function of the reactant of an N type MIS transistor become smaller than the work function of the reactant of a P type MIS transistor.
[0136] Next, an example of the production process is explained with reference to drawing 19 (a) - Fig. 1919 (c) about the 3rd example concerning the 3rd operation gestalt of this invention.
[0137] In addition, since it is the same as that of the 1st example which the intermediate process (process of drawing 15 (a) - drawing 16 (d)) mentioned above, this example explains the process after the process of drawing 16 (d).
[0138] After the process of drawing 16 (e), a spatter and the CMP method are used for the slot for gate electrode formation, and the nickel (nickel) film 331 is embedded as a gate electrode material of a P type MIS transistor in it (drawing 19 (a)).
[0139] Next, after depositing the amorphous silicon (a-Si) film 332 on the whole surface by a spatter etc., the amorphous silicon film 332 of fields other than on an N type MIS transistor field is removed using the photolithography method, the dry etching method, etc. (drawing 19 (b)).
[0140] Next, by adding 400 degrees C and heat treatment for about 1 minute, in the gate electrode section of an N type MIS transistor field, the nickel film 331 and the amorphous silicon film 332 are made to react, and the nickel silicide (NiSi) film 333 is formed. Then, isotropic etching, such as chemical dry etching, removes the amorphous silicon film 332 which was not contributed to a reaction. Thus, by changing the nickel film 331 to the

nickel silicide film 333, the work function of an ingredient can be reduced to about 4.36eV from about 5.0eV (drawing 19 (c)).

[0141] Finally, the MIS transistor transistor of N type and P type is completed like the 1st example by depositing an interlayer insulation film, making the hole for contact, and forming wiring further.

[0142] In addition, in the example mentioned above, the gate electrode of a P type MIS transistor may be formed by cobalt (Co), cobalt silicide (CoSi2), chromium (Cr) and chromium silicide (CrSi2), molybdenum (Mo), molybdenum silicide (MoSi2), etc., although nickel (nickel) and the gate electrode of an N type MIS transistor were made into nickel silicide (NiSi and NiSi2).

[0143] Since the work function of the part which touches the gate dielectric film of an N type MIS transistor can be made smaller than the work function of the part which touches the gate dielectric film of a P type MIS transistor according to this operation gestalt, it is possible to optimize the work function of the gate electrode of N type and each P type MIS transistor, and to optimize the threshold electrical potential difference of both transistors. Moreover, since etching removal of the metal membrane formed in Mizouchi for gate electrode formation is not carried out like before with this operation gestalt, it is possible to control the fall of the dependability of gate dielectric film.

[0144] As mentioned above, although the operation gestalt of this invention was explained, it is possible for this invention to deform within limits which are not limited to the above-mentioned operation gestalt and do not deviate from the meaning variously, and to carry out.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 2] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 3] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 4] The top view having shown the effectiveness acquired by the manufacture approach of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 5] Drawing having shown the distance dependency between components of the threshold as contrasted with the conventional technique about the MIS transistor obtained by the manufacture approach of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 6] Drawing having shown typically an example of the basic configuration of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 7] Drawing having shown typically other examples of the basic configuration of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 8] Drawing having shown typically other examples of the basic configuration of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 9] Drawing having shown typically other examples of the basic configuration of the semiconductor device concerning the 1st operation gestalt of this invention.
[Drawing 10] Drawing having shown the main production processes for obtaining the basic configuration shown in drawing 8 .
[Drawing 11] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 12] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 13] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 14] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the 2nd operation gestalt of this invention.
[Drawing 15] The process sectional view having shown a part of the process about an example of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 16] The process sectional view having shown a part of the process about an example of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 17] The process sectional view having shown a part of the process about an example of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 18] The process sectional view having shown a part of the process about other examples of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 19] The process sectional view having shown a part of the process about other examples of the manufacture approach of the semiconductor device concerning the 3rd operation gestalt of this invention.
[Drawing 20] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the conventional technique.

[Drawing 21] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the conventional technique.
[Drawing 22] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the conventional technique.
[Drawing 23] The process sectional view having shown a part of the process about the manufacture approach of the semiconductor device concerning the conventional technique.
[Drawing 24] The top view having shown the trouble of the manufacture approach of the semiconductor device concerning the conventional technique.
[Description of Notations]
101 -- Silicon substrate
102 -- Isolation
103 -- Silicon oxide
104 -- Polish recon film
105 107 -- Silicon nitride
106 108 -- Source drain diffusion layer
109 -- Silicide film
110 -- Interlayer insulation film
111 -- Slot
112 -- Hafnium oxide film
113 -- Hafnium nitride
114 -- Resist
115 -- Cobalt film
201 -- Silicon substrate
202, 205, 206, 207 -- Silicon oxide
203 214 -- Silicon nitride
204 215 -- Resist
208 -- Polish recon film
209 -- Source drain diffusion layer
210 218 -- Interlayer insulation film
211 -- Slot
212 -- Ta 2O5 Film
213 -- Ru film or Pd film
216 -- In film or Sn film
217 -- Tungsten film
219 -- Wiring
301 -- Silicon substrate
302 -- Isolation
303 -- P type -- a well
304 -- N type -- a well
305 312 -- Silicon oxide
306 -- Polish recon film
307 309 -- Source drain diffusion layer
308 314 -- Silicon nitride
310 317 -- Interlayer insulation film
311 -- Slot
313 -- Tungsten silicide film
315 -- Palladium film
316 -- Palladium silicide film
318 -- Wiring
321 322 -- Resist
323 -- Germanium film
324 -- Indium film
331 -- Nickel film
332 -- Amorphous silicon film

333 -- Nickel silicide film

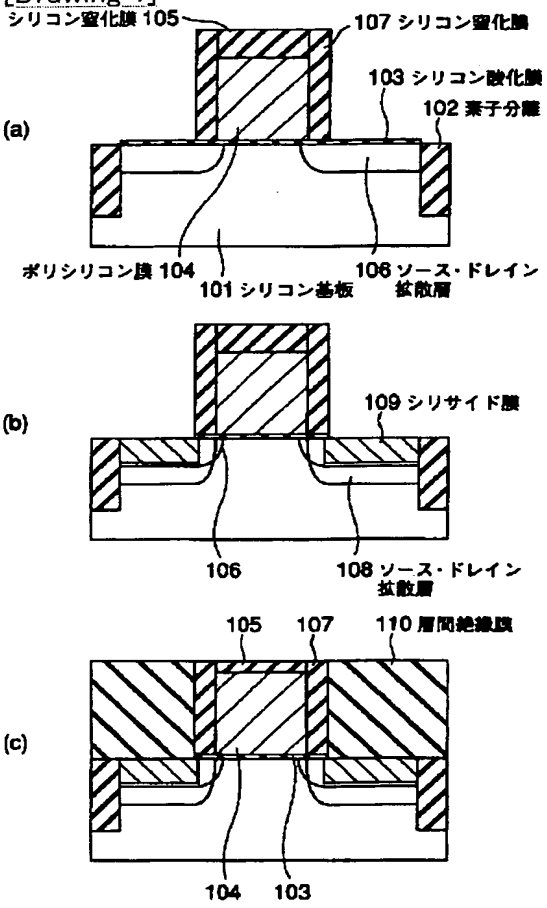
[Translation done.]

* NOTICES *

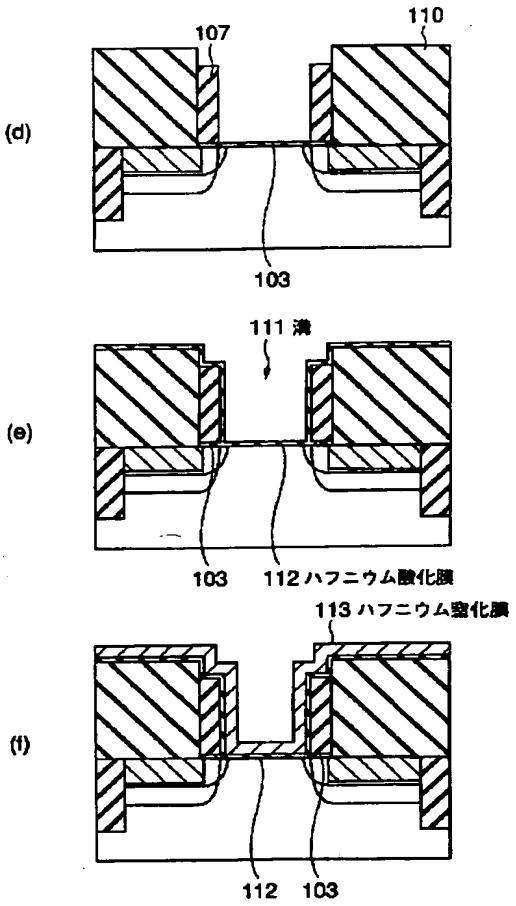
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

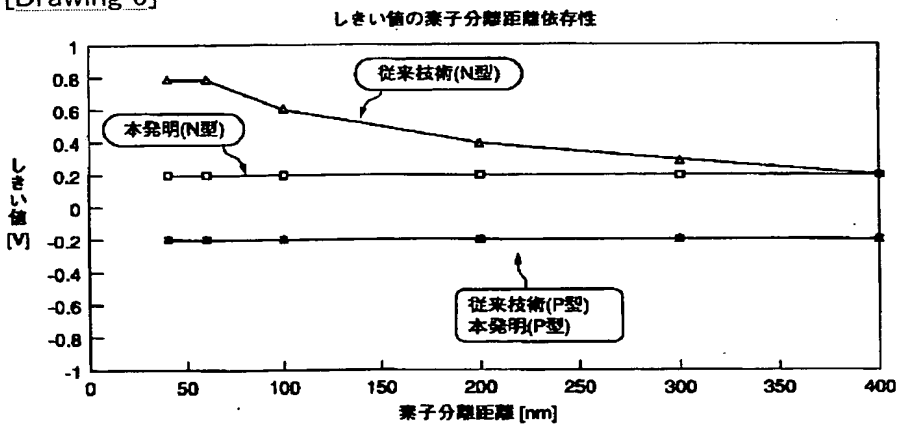
[Drawing 1]



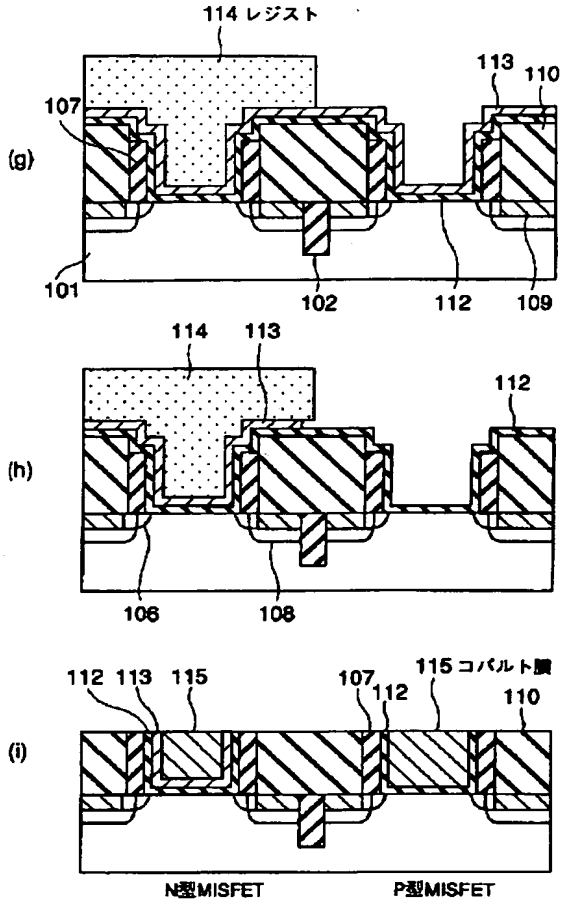
[Drawing 2]



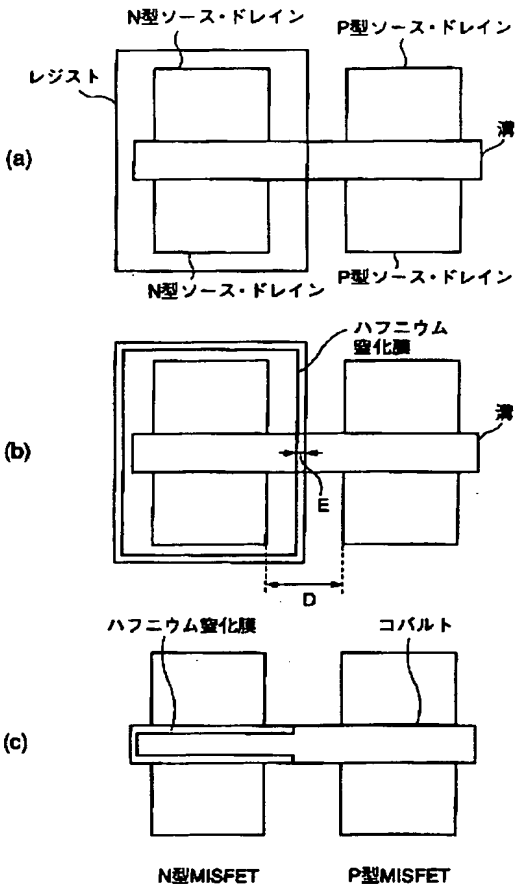
[Drawing 5]



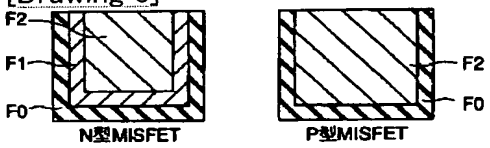
[Drawing 3]


(g)
114 レジスト
113
110
107
101
102
112
109
(h)
114
113
112
106
108
(i)
112 113 115
107
112
115 コバルト膜
110
N型MISFET
P型MISFET

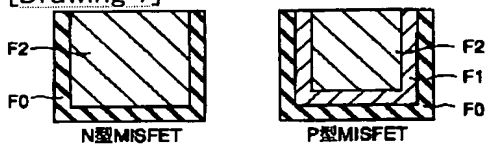
[Drawing 4]



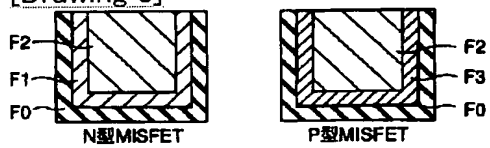
[Drawing 6]



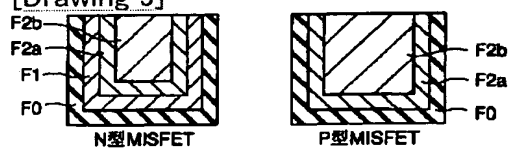
[Drawing 7]



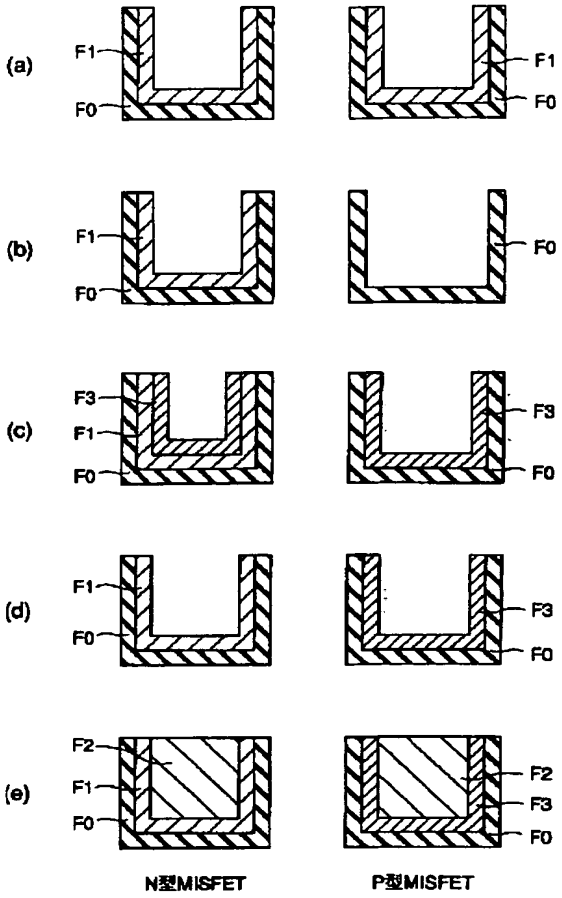
[Drawing 8]



[Drawing 9]



[Drawing 10]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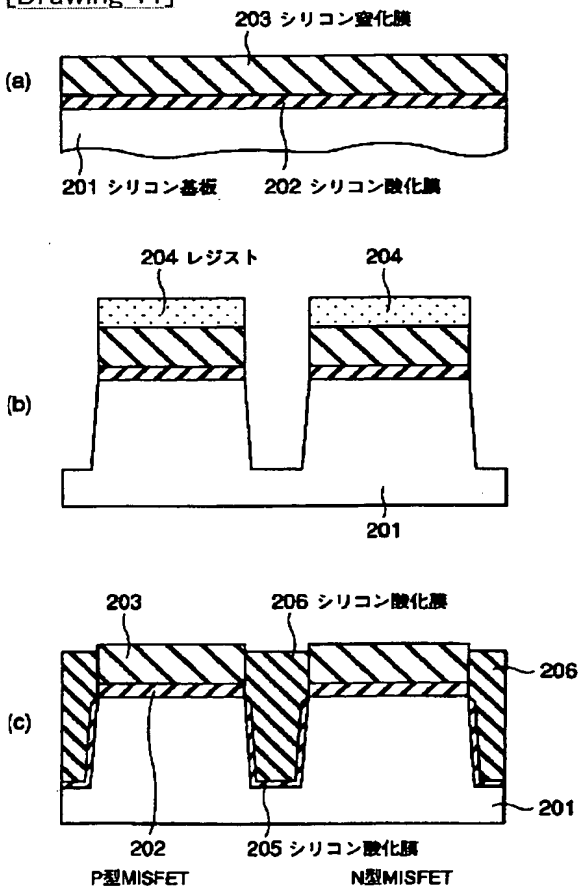
F1
F0
F1
F0
(b)
F1
F0
F0
(c)
F3
F1
F0
F3
F0
(d)
F1
F0
F3
F0
(e)
F2
F1
F0
F2
F3
F0
N型MISFET
P型MISFET

[Drawing 11]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201 シリコン基板
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(b)
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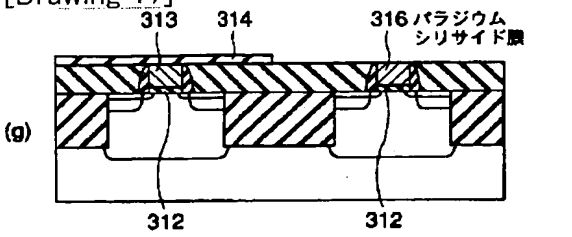
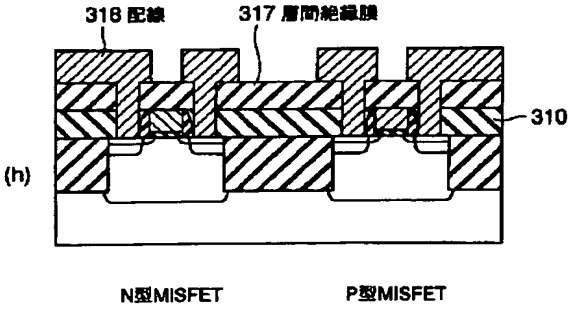
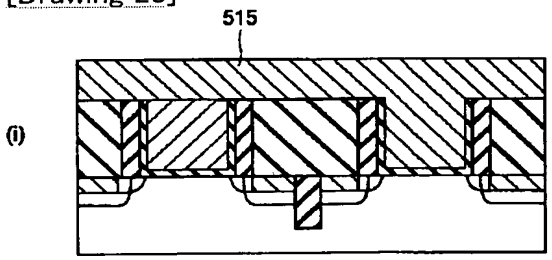
204
201
(c)
203
206 シリコン酸化膜
206
201
202
P型MISFET
205 シリコン酸化膜
N型MISFET

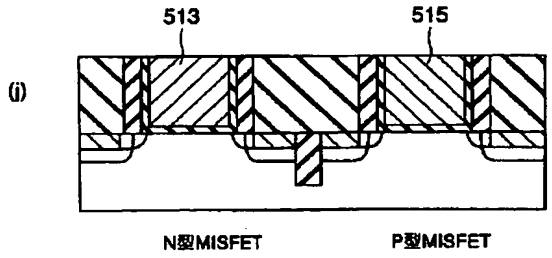
[Drawing 17]



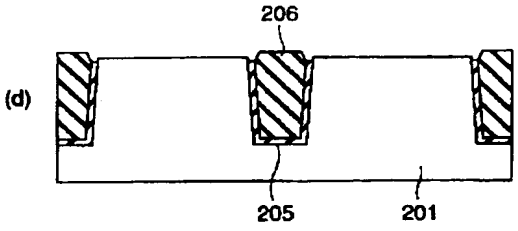


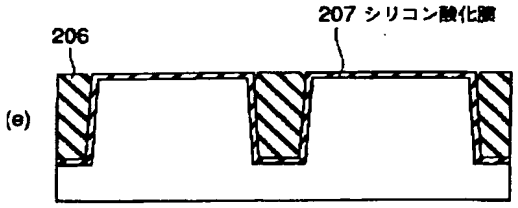
[Drawing 23]

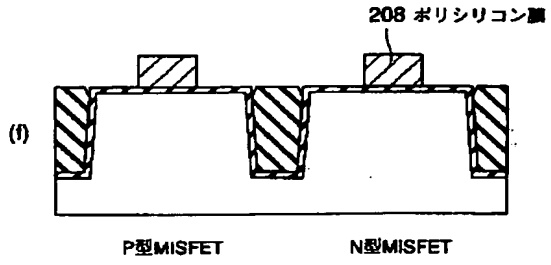




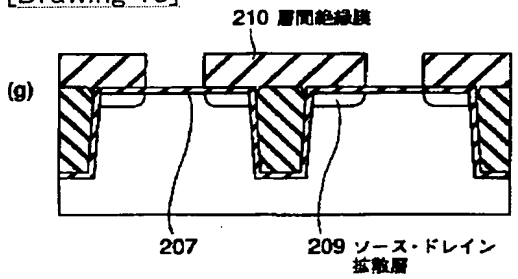
[Drawing 12]

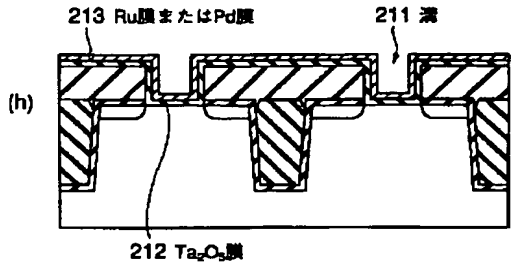

206
(d)
205
201

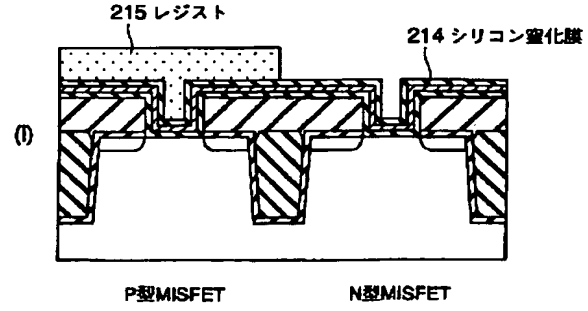

207 シリコン酸化膜
206
(e)


208 ポリシリコン膜
(f)
P型MISFET
N型MISFET

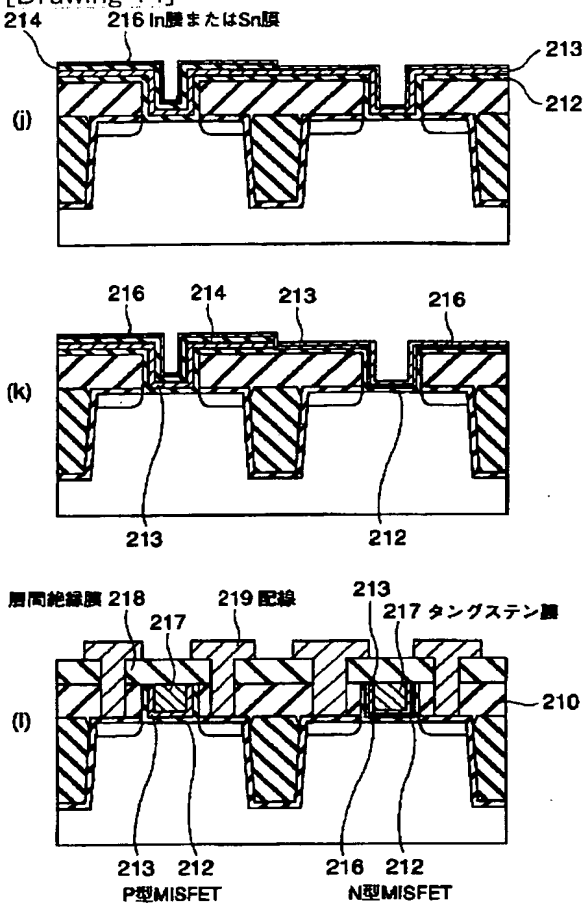
[Drawing 13]


210 層間絶縁膜
(g)
207
209 ソース・ドレイン
拡散層

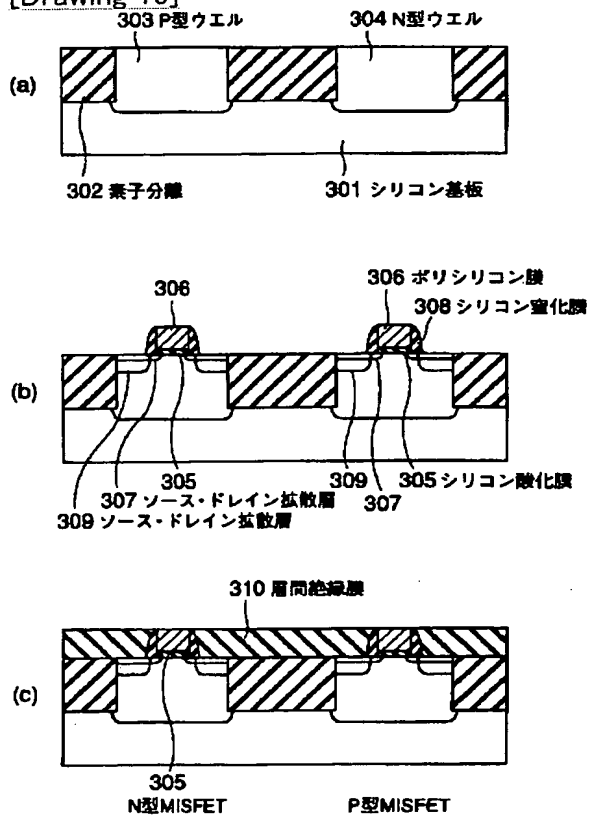

213 Ru膜またはPd膜
211 溝
(h)
212 Ta2O5膜


215 レジスト
214 シリコン窒化膜
(i)
P型MISFET
N型MISFET

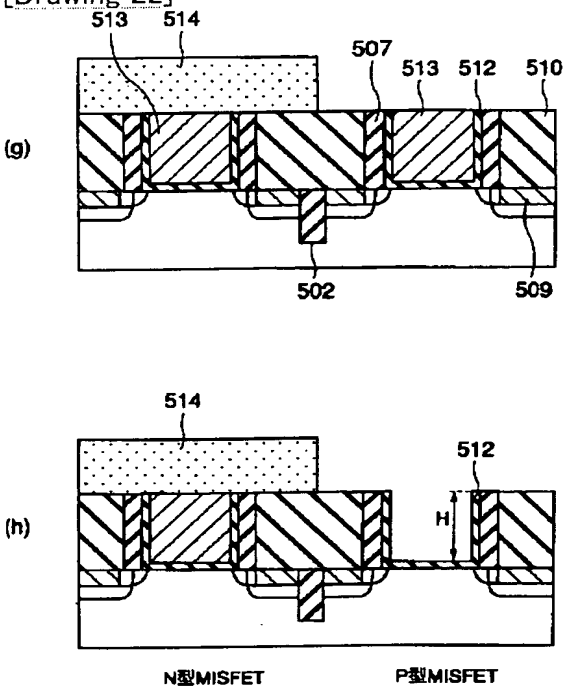
[Drawing 14]



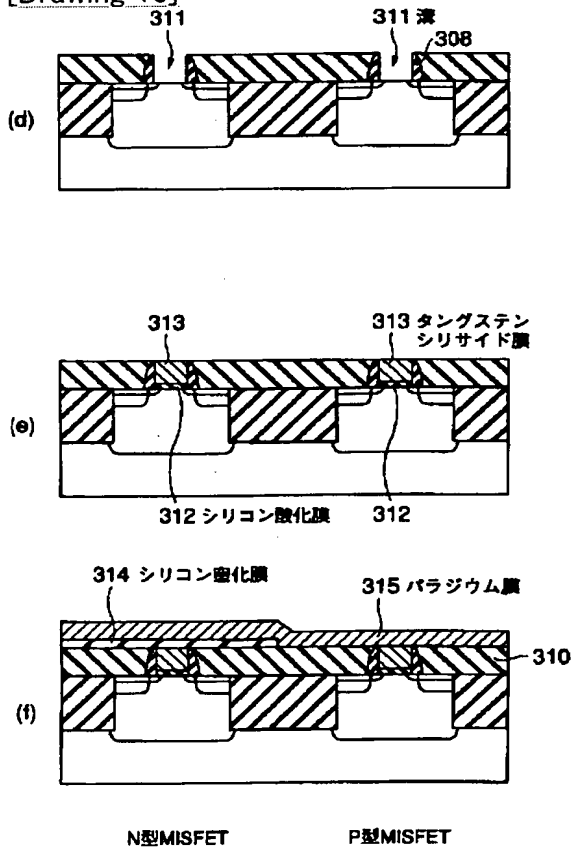
[Drawing 15]



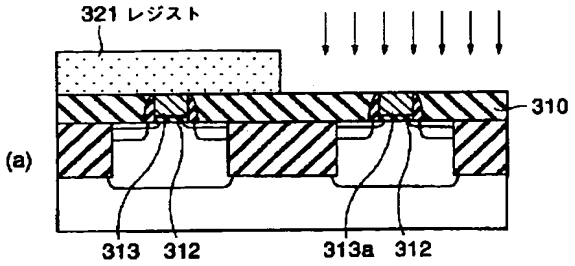
[Drawing 22]

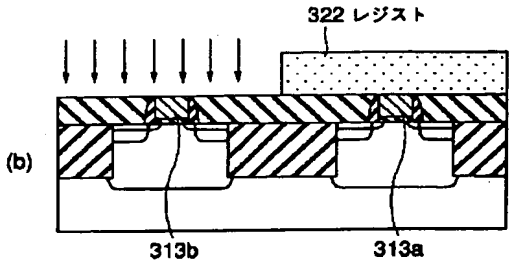


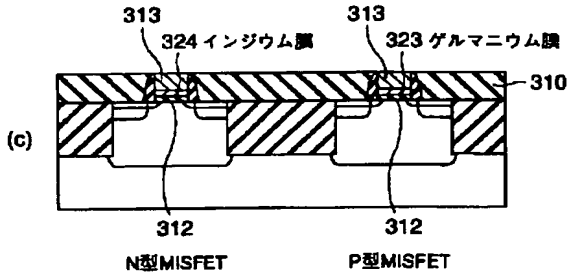
[Drawing 16]



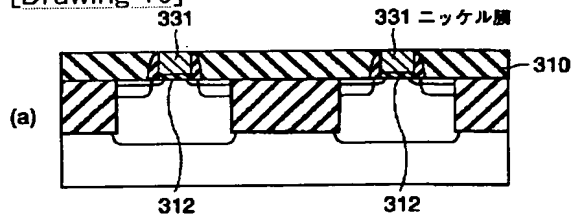
[Drawing 18]

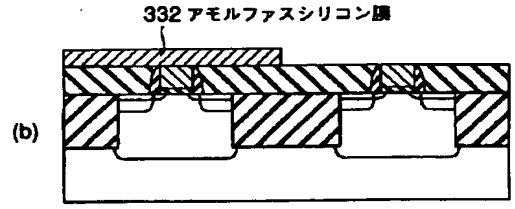

321 レジスト
310
(a)
313
312
313a
312

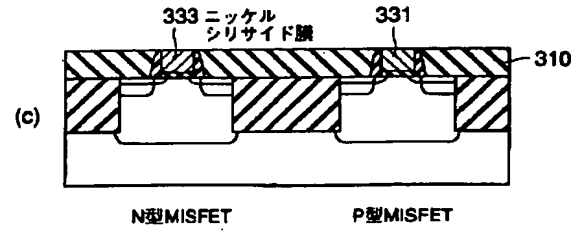

322 レジスト
(b)
313b
313a


313
324 インジウム膜
313
323 ゲルマニウム膜
310
(c)
312
312
N型MISFET
P型MISFET

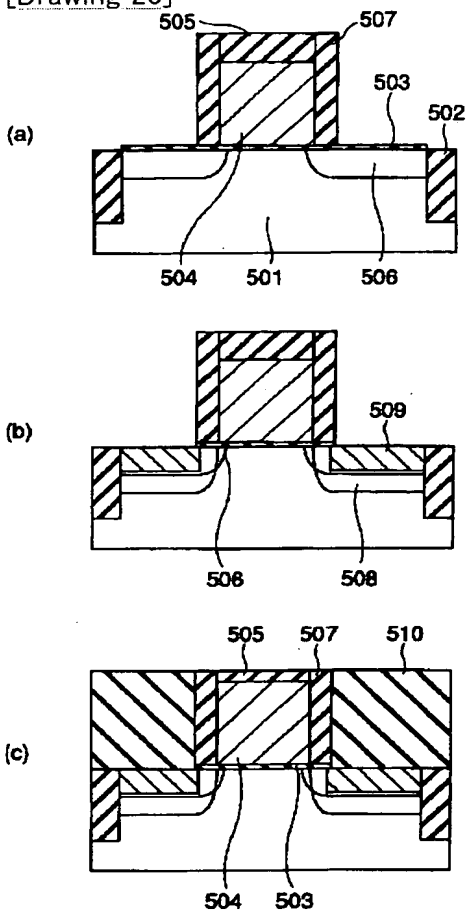
[Drawing 19]


331
331 ニッケル膜
310
(a)
312
312

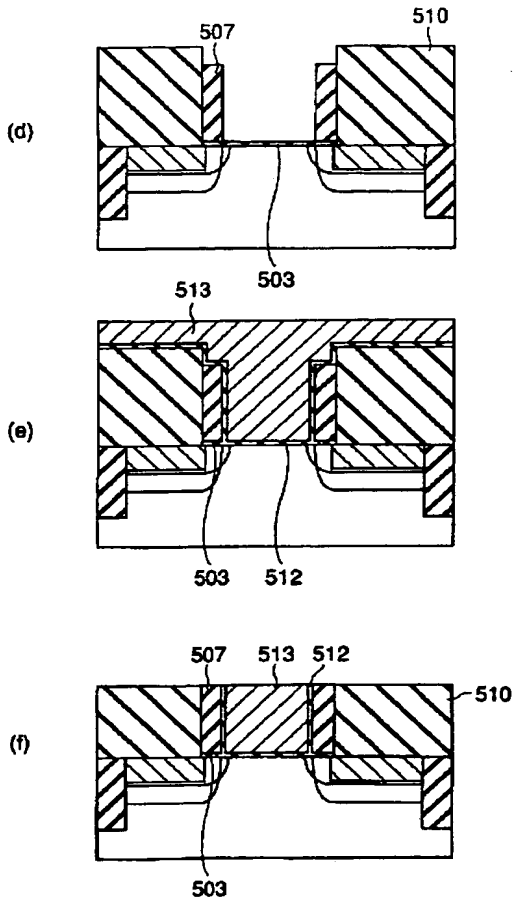

332 アモルファスシリコン膜
(b)


333 ニッケル
シリサイド膜
331
310
(c)
N型MISFET
P型MISFET

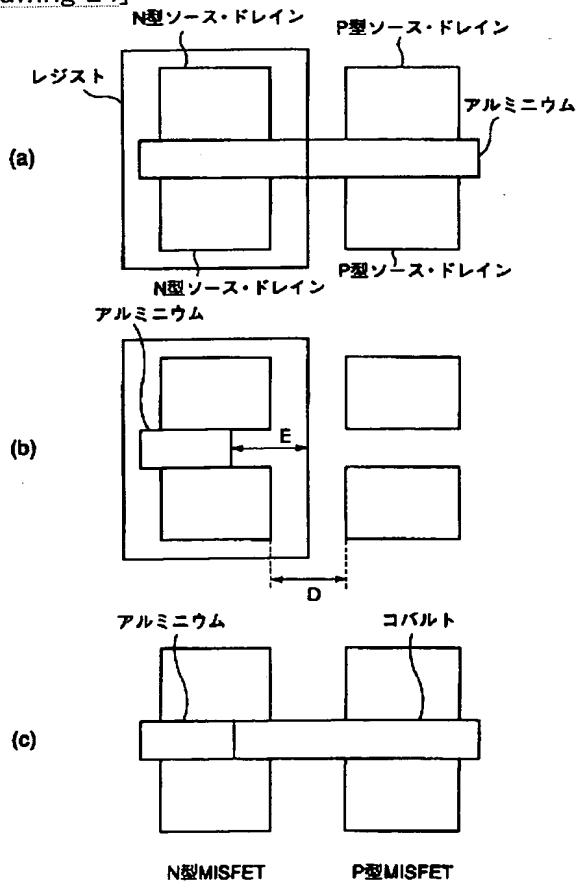
[Drawing 20]



[Drawing 21]


(d)
507
510
503
(e)
513
503
512
(f)
507
513
512
510
503

[Drawing 24]


N型ソース・ドレイン
P型ソース・ドレイン
レジスト
アルミニウム
(a)
N型ソース・ドレイン
P型ソース・ドレイン
アルミニウム
(b)
E
D
アルミニウム
コバルト
(c)
N型MISFET
P型MISFET

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) 公開特許公報（Ａ）　(11)特許出願公開番号
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(51)Int.Cl.'	識別記号	ＦＩ		テーマコード'（参考）
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21/8238		27/08	３２１Ｄ	５Ｆ０４０
27/092		29/62	Ｇ	５Ｆ０４８
29/43				

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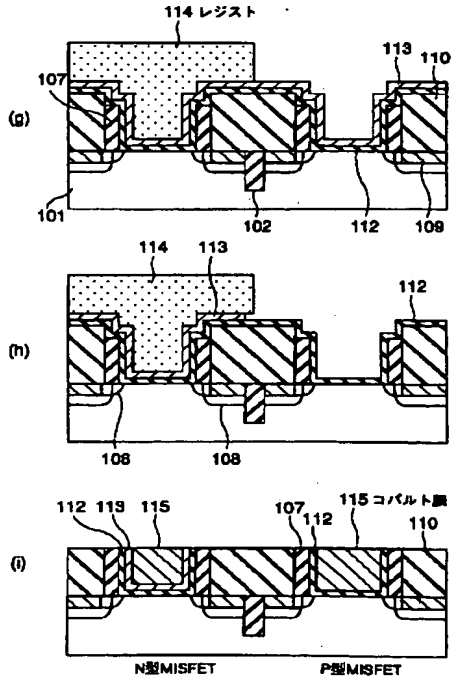
最終頁に続く

(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】
・【課題】　ダマシンゲート技術等を用いてゲート電極を作製する場合に、半導体装置の微細化等を可能にする。
・【解決手段】　ゲート電極を形成する工程が、Ｎ型及びＰ型ＭＩＳトランジスタ領域の凹部内に第１の金属含有膜１１３を形成する工程と、Ｐ型ＭＩＳトランジスタ領域に形成された第１の金属含有膜を除去する工程と、Ｎ型ＭＩＳトランジスタ領域に残置した第１の金属含有膜上及びＰ型ＭＩＳトランジスタ領域のゲート絶縁膜１１２上に第２の金属含有膜１１５を形成する工程とからなり、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する金属含有膜の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する金属含有膜の仕事関数よりも小さい。



1

·【特許請求の範囲】
·【請求項１】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極が半導体基板に形成された凹部内にゲート絶縁膜を介して形成されている半導体装置であって、
Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタの少なくとも一方のゲート電極は複数の金属含有膜の積層構造によって構成され、かつＮ型ＭＩＳトランジスタのゲート絶縁膜に接する金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置。
·【請求項２】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、
Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、
第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜を除去する工程と、
第１又は第２のゲート形成領域の他方の領域に残置した第１の金属含有膜上及び第１又は第２のゲート形成領域の一方の領域のゲート絶縁膜上に第２の金属含有膜を形成することにより第１及び第２のゲート形成領域の双方の領域の凹部を埋め込む工程とからなり、
前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置の製造方法。
·【請求項３】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、
Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、
第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜を除去する工程と、
第１又は第２のゲート形成領域の他方の領域に残置した第１の金属含有膜上及び第１又は第２のゲート形成領域の一方の領域のゲート絶縁膜上に第３の金属含有膜を形成する工程と、

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第１又は第２のゲート形成領域の他方の領域に形成された第３の金属含有膜を除去する工程と、
第１又は第２のゲート形成領域の一方の領域に残置した第３の金属含有膜上及び第１又は第２のゲート形成領域の他方の領域に露出した第１の金属含有膜上に第２の金属含有膜を形成することにより第１及び第２のゲート形成領域の双方の領域の凹部を埋め込む工程とからなり、
前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置の製造方法。
·【請求項４】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、
Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、
第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第２の金属含有膜に変換する工程とからなり、
前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置の製造方法。
·【請求項５】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、
Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、
第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第２の金属含有膜に変換する工程と、
第１又は第２のゲート形成領域の他方の領域に形成された第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第３の金属含有膜に変換する工程とからなり、
前記第２及び第３の金属含有膜のうち、Ｎ型ＭＩＳトラ

シジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置の製造方法。

・【請求項６】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、

Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、

第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜中を該第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第２の金属含有膜を形成する工程とからなり、

前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置の製造方法。

・【請求項７】Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、

Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、

第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜中を該第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第２の金属含有膜を形成する工程と、

第１又は第２のゲート形成領域の他方の領域に形成された第１の金属含有膜中を該第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第３の金属含有膜を形成する工程とからなり、

前記第２及び第３の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする半導体装置の製造方法。

・【発明の詳細な説明】

・【０００１】

・【発明の属する技術分野】本発明は、半導体装置及びその製造方法、特にＮ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタのゲート電極の改良に関するものである。

・【０００２】

・【従来の技術】ＭＩＳトランジスタの高性能化のためには、素子の微細化が必須である。しかし、ゲート絶縁膜として現在用いられているシリコン酸化膜は、誘電率が低いため、ゲート絶縁膜の容量を大きくできないという問題がある。また、ゲート電極として用いられているポリシリコンは、抵抗率が高いため、低抵抗化を達成できないという問題がある。それぞれの問題に対して、ゲート絶縁膜には高誘電体材料を用い、ゲート電極には金属材料を用いるという提案がなされている。

・【０００３】ところが、これらの材料は、現在用いられている材料に比べて耐熱性に劣るという欠点を有している。そこで、高温プロセスを行った後にゲート絶縁膜及びゲート電極を形成することが可能な技術として、ダマシンゲート技術が提案されている。

・【０００４】ダマシンゲート技術は、ゲート形成予定領域に予めダミーとなるゲートを形成しておき、ソース・ドレイン拡散層を形成した後にダミーゲートを除去し、ダミーゲートを除去した領域に電極材料を埋め込んでゲート電極を作製するものである。

・【０００５】ダマシーンゲート技術を用いてゲート電極を作製する場合、Ｎ型及びＰ型ＭＩＳトランジスタのゲート電極に同一の金属を用いると、両トランジスタのゲート電極の仕事関数を異ならせることができないため、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのしきい値を適正化することができない。

・【０００６】したがって、Ｎ型ＭＩＳトランジスタとＰ型ＭＩＳトランジスタとで、異なるゲート電極材料を用いる製造プロセスが必要とされる。以下、このような製造プロセスの一例について、図２０（ａ）～図２３・（ｉ）を参照して説明する。

・【０００７】まず、シリコン基板５０１上にＳＴＩ構造の素子分離５０２を形成する。続いて、将来除去されるダミー絶縁膜として、膜厚６ｎｍ程度のシリコン酸化膜５０３を形成する。さらに、将来除去されるダミーゲートとして、膜厚１５０ｎｍ程度のポリシリコン膜５０４及び膜厚５０ｎｍ程度のシリコン窒化膜５０５の積層構造を形成する。これらのダミー絶縁膜及びダミーゲートは、通常の技術（酸化やＣＶＤ等の成膜技術、リソグラフィー技術、ＲＩＥ技術等）を用いて形成する。続いて、ダミーゲート（ポリシリコン膜５０４及びシリコン窒化膜５０５）をマスクとして、イオン注入技術により、ソース・ドレイン拡散層５０６となるエクステンション用の不純物拡散層を形成する。続いて、シリコン窒化膜５０７からなる幅４０ｎｍ程度のゲート側壁絶縁膜

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を、ＣＶＤ技術とＲＩＥ技術によって形成する（図２０（ａ））。

【０００８】次に、ダミーゲート（ポリシリコン膜５０４及びシリコン窒化膜５０５）及びゲート側壁絶縁膜（シリコン窒化５０７）をマスクとして、イオン注入技術により、ソース・ドレイン拡散層５０８となる高濃度不純物拡散層を形成する。さらに、サリサイドプロセス技術により、ダミーゲートをマスクとしてソース・ドレイン領域のみに厚さ４０ｎｍ程度のシリサイド膜（コバルト或いはチタン等のシリサイド）５０９を形成する（図２０（ｂ））。

【０００９】次に、層間絶縁膜５１０として、例えばシリコン酸化膜をＣＶＤ法により堆積する。さらに、この層間絶縁膜５１０をＣＭＰ技術によって平坦化することにより、シリコン窒化膜５０５及び５０７の表面を露出させる（図２０（ｃ））。

【００１０】次に、例えば燐酸を用いて、ダミーゲート上部のシリコン窒化膜５０５を層間絶縁膜５１０に対して選択的に除去する。このときに、シリコン窒化膜５０７もポリシリコン膜５０４の高さ程度までエッチングされる。続いて、例えばフッ素などのハロゲン原子のラジカルを用いたエッチング技術により、ポリシリコン膜５０４を層間絶縁膜５１０及びシリコン窒化膜５０７に対して選択的に除去する（図２１（ｄ））。

【００１１】次に、フッ酸等のウエットエッチングによりダミーのシリコン酸化膜５０３を除去することにより、溝（凹部）が形成される。続いて、ゲート絶縁膜として、高誘電体絶縁膜であるTa_2O_5膜５１２を、例えばＣＶＤ法等によって形成する。続いて、ゲート電極として、例えばアルミニウム膜５１３を堆積する（図２１（ｅ））。

【００１２】次に、ＣＭＰ技術を用いて、Ta_2O_5膜５１２及びアルミニウム膜５１３の平坦化を、層間絶縁膜５１０が露出するまで行う（図２１（ｆ））。

【００１３】以上の図２０（ａ）～図２１（ｆ）の工程は、Ｎ型ＭＩＳトランジスタ形成領域及びＰ型ＭＩＳトランジスタ形成領域の双方に対して行われるが、図面上では一方の領域のみを示した。以後の工程からは、Ｎ型ＭＩＳトランジスタ（Ｎ型ＭＩＳＦＥＴ）形成領域及びＰ型ＭＩＳトランジスタ（Ｐ型ＭＩＳＦＥＴ）形成領域の双方を図面上に示す。

【００１４】図２１（ｆ）の工程の後、リソグラフィー技術を用いて、Ｐ型ＭＩＳトランジスタ形成領域以外をレジスト５１４で覆う（図２２（ｇ））。

【００１５】次に、燐酸によるウエットエッチングを行うことにより、Ｐ型領域のみアルミニウム膜５１３を除去する。この時、シリコン窒化膜５０７が露出しているが、室温の燐酸ではほとんどエッチングされない（図２２（ｈ））。

【００１６】次に、レジスト５１４を除去した後、仕事

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関数が５ｅＶ程度となる金属として、例えばコバルト膜５１５を全面に堆積する（図２３（ｉ））。

【００１７】次に、ＣＭＰ技術を用いて、コバルト膜５１５の平坦化を、層間絶縁膜５１０が露出するまで行う（図２３（ｊ））。

【００１８】以上の工程により、ゲート電極構造として、Ｎ型はアルミニウム膜５１３からなり、Ｐ型はコバルト膜５１５からなるＣ－ＭＩＳトランジスタが完成する。アルミニウム膜５１３は仕事関数が４．２ｅＶ程度、コバルト膜５１５は仕事関数が５ｅＶ程度であるため、Ｎ型ＭＩＳトランジスタとＰ型ＭＩＳトランジスタとで、それぞれでゲート電極の仕事関数を最適化することができ、両トランジスタのしきい値電圧を最適化することができる。

【００１９】しかしながら、上述した従来技術では、微細化に対して大きな問題が生じる。以下、この問題について説明する。

【００２０】図２４（ａ）、図２４（ｂ）及び図２４（ｃ）は、それぞれ図２２（ｇ）、図２２（ｈ）及び図２３（ｊ）における主要部を模式的に示した平面図である。Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタのそれぞれのソース・ドレイン間の距離、すなわち素子間距離をＤとする。

【００２１】図２２（ｈ）の工程において、レジスト５１４をマスクにしてＰ型領域のアルミニウム膜５１３をウエットエッチングすると、ウエットエッチングは等方的に進行する。そのため、レジスト５１４でマスクされた領域までエッチングが深く進み、図２４（ｂ）に示すように、Ｎ型領域までアルミニウム膜５１３がエッチングされてしまう。

【００２２】したがって、完成されたトランジスタ構造は、図２４（ｃ）に示すようになる。すなわち、Ｎ型領域では、仕事関数が互いに異なるアルミニウム膜とコバルト膜によってゲート電極が構成されることになる。そのため、Ｎ型ＭＩＳトランジスタでは、しきい値の異なる領域が存在することになり、低いしきい値電圧の設定が望めなくなる。

【００２３】上述した問題についてさらに検討する。ウエットエッチングによる横方向のエッチング量Ｅは、通常エッチングされるアルミニウム膜の高さＨ（図２２（ｈ）参照）以上となる。上述した例では、アルミニウム膜の高さＨは１５０ｎｍ程度であるため、横方向のエッチング量Ｅは１５０ｎｍ以上となる。したがって、上述した問題を避けるためには、素子間距離Ｄを横方向のエッチング量Ｅの２倍以上、すなわち３００ｎｍ以上にすることが必要となり、微細化を行うことが極めて困難になる。アルミニウム膜の高さＨを低くすることである程度の微細化が可能になるが、アルミニウム膜の高さＨの減少によってゲート抵抗が増大するため、本質的な解決策とはならない。

・【００２４】また、上述した従来技術では、ゲート絶縁膜等の信頼性に対しても大きな問題が生じる。以下、この問題について説明する。

・【００２５】上述した従来技術では、図２２（ｈ）の工程において、Ｐ型領域のアルミニウム膜５１３をウエットエッチングで除去した後、除去した領域に図２３（ｉ）及び（ｊ）の工程でコバルト膜５１５を形成する。したがって、アルミニウム膜５１３のエッチング等によってゲート絶縁膜５１２の表面が劣化し、ゲート絶縁膜の信頼性に対して悪影響が生じることになる。

・【００２６】

・【発明が解決しようとする課題】以上述べたように、従来のダマシンゲート技術では、ダミーゲートをエッチング除去する際に、エッチングが横方向に深く進行するため、微細化が困難であるという問題があった。また、ダミーゲートをエッチング除去することによって、ゲート絶縁膜等の信頼性に悪影響を与えるという問題もあった。

・【００２７】本発明は、上記従来の問題に対してなされたものであり、ダマシンゲート技術等を用いてゲート電極が作製される半導体装置において、半導体装置の微細化を達成することを第１の目的とし、ゲート電極等の信頼性を確保することを第２の目的とする。

・【００２８】

・【課題を解決するための手段】本発明（発明Ａ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極が半導体基板に形成された凹部内にゲート絶縁膜を介して形成されている半導体装置であって、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタの少なくとも一方のゲート電極は複数の金属含有膜の積層構造によって構成され、かつＮ型ＭＩＳトランジスタのゲート絶縁膜に接する金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数（Ｗ１）がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数（Ｗ２）よりも小さいことを特徴とする。

・【００２９】本発明（発明Ｂ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜を除去する工程と、第１又は第２のゲート形成領域の他方の領域に残置した第１の金属含有膜上及び第１又は第２のゲート形成領域の一方の領域のゲート絶縁膜上に第２の金属含有膜を形成することにより第１及び第２のゲート形成領域の双方の領域の凹部を埋め込む工程とからなり、前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数（Ｗ１）がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数（Ｗ２）よりも小さいことを特徴とする。

・【００３０】本発明（発明Ｃ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜を除去する工程と、第１又は第２のゲート形成領域の他方の領域に残置した第１の金属含有膜上及び第１又は第２のゲート形成領域の一方の領域のゲート絶縁膜上に第３の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の他方の領域に形成された第３の金属含有膜を除去する工程と、第１又は第２のゲート形成領域の一方の領域に残置した第３の金属含有膜上及び第１又は第２のゲート形成領域の他方の領域に露出した第１の金属含有膜上に第２の金属含有膜を形成することにより第１及び第２のゲート形成領域の双方の領域の凹部を埋め込む工程とからなり、前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数（Ｗ１）がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数（Ｗ２）よりも小さいことを特徴とする。

・【００３１】本発明（発明Ａ、Ｂ、Ｃ）によれば、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数よりも小さいため、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのゲート電極の仕事関数を最適化することができ、Ｎ型及びＰ型ＭＩＳトランジスタのしきい値電圧を最適化することが可能である。

・【００３２】また、本発明（発明Ａ、Ｂ、Ｃ）によれば、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタの少なくとも一方のゲート電極は複数の金属含有膜で形成されているため、ゲート絶縁膜に接する部分の膜の抵抗率が低くなくても、上層側に抵抗率の低い膜を設けることで、ゲート電極全体の抵抗を低くすることができる。

・【００３３】また、本発明（発明Ｂ、Ｃ）によれば、第１、第３の金属含有膜上に第２の金属含有膜を形成するので、第１、第３の金属含有膜の膜厚を薄くすることが

できる。したがって、第１又は第２のゲート形成領域の一方の領域に形成された金属含有膜（第１、第３の金属含有膜）を除去する際に、第１又は第２のゲート形成領域の他方の領域まで深くエッチングが進行することを防止でき、半導体装置の微細化を達成することが可能となる。

【００３４】なお、本発明（発明Ａ、Ｂ、Ｃ）では、仕事関数Ｗ１が半導体基板に用いる半導体のバンドギャップの中央（バンドギャップの１／２の位置）よりも伝導帯に近い側にあり、仕事関数Ｗ２がバンドギャップの中央よりも荷電子帯に近い側にあることが好ましい。また、ＭＩＳトランジスタのしきい値を決めるゲート絶縁膜に接する領域の厚さは、所望のしきい値が得られる厚さ以上であればよいが、好ましくは１０原子層程度以上となるようにする。

【００３５】また、本発明（発明Ａ、Ｂ、Ｃ）では、Ｎ型及びＰ型ＭＩＳトランジスタのゲート絶縁膜に接するそれぞれの部分は、必ずしも異種の材料である必要はなく、同種の材料であっても両者間で組成或いは結晶構造を異ならせることにより、両者の仕事関数を異ならせることができるものであればよい。

【００３６】本発明（発明Ｄ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第２の金属含有膜に変換する工程とからなり、前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする。

【００３７】本発明（発明Ｅ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第２の金

属含有膜に変換する工程と、第１又は第２のゲート形成領域の他方の領域に形成された第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第３の金属含有膜に変換する工程とからなり、前記第２及び第３の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする。

【００３８】本発明（発明Ｆ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜中を該第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第２の金属含有膜を形成する工程とからなり、前記第１及び第２の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする。

【００３９】本発明（発明Ｇ）は、Ｎ型ＭＩＳトランジスタ及びＰ型ＭＩＳトランジスタそれぞれのゲート電極を半導体基板に形成された凹部内にゲート絶縁膜を介して形成する半導体装置の製造方法であって、前記ゲート電極を形成する工程は、Ｎ型ＭＩＳトランジスタ用の第１のゲート形成領域及びＰ型ＭＩＳトランジスタ用の第２のゲート形成領域の双方の領域の凹部内に形成されたゲート絶縁膜上に第１の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の一方の領域に形成された第１の金属含有膜中を該第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第２の金属含有膜を形成する工程と、第１又は第２のゲート形成領域の他方の領域に形成された第１の金属含有膜中を該第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第３の金属含有膜を形成する工程とからなり、前記第２及び第３の金属含有膜のうち、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する方の金属含有膜の少なくともゲート絶縁膜に接する部分の仕事関数よりも小さいことを特徴とする。

・【００４０】本発明（発明D、E、F、G）によれば、N型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数がＰ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数よりも小さいため、N型及びＰ型ＭＩＳトランジスタそれぞれのゲート電極の仕事関数を最適化することができ、N型及びＰ型ＭＩＳトランジスタのしきい値電圧を最適化することが可能である。

・【００４１】また、本発明（発明D、E、F、G）によれば、第１の金属含有膜に含まれる物質と該物質以外の物質とを反応させることにより第１の金属含有膜を第２、第３の金属含有膜に変換する、或いは、第１の金属含有膜中を第１の金属含有膜に含まれる物質以外の物質を拡散させてゲート絶縁膜界面に析出させることにより第２、第３の金属含有膜を形成するので、凹部内のゲート絶縁膜上に形成された金属含有膜をエッチングしないでゲート電極を作製することができ、ゲート絶縁膜の信頼性の低下を防止することが可能である。

・【００４２】なお、本発明（発明D、E、F、G）では、仕事関数Ｗ１が半導体基板に用いる半導体のバンドギャップの中央（バンドギャップの１／２の位置）よりも伝導帯に近い側にあり、仕事関数Ｗ２がバンドギャップの中央よりも荷電子帯に近い側にあることが好ましい。また、ＭＩＳトランジスタのしきい値を決めるゲート絶縁膜に接する領域の厚さは、所望のしきい値が得られる厚さ以上であればよいが、好ましくは１０原子層程度以上となるようにする。

・【００４３】

・【発明の実施の形態】以下、本発明の実施形態を図面を参照して説明する。

・【００４４】（実施形態１）以下、本発明の第１の実施形態に係る製造工程の一例について、図１（ａ）～図３・（ｉ）を参照して説明する。

・【００４５】まず、シリコン基板１０１上にＳＴＩ構造の素子分離１０２を形成する。続いて、将来除去されるダミー絶縁膜として、膜厚２～６ｎｍ程度のシリコン酸化膜１０３を形成する。さらに、将来除去されるダミーゲートとして、膜厚１５０ｎｍ程度のポリシリコン膜１０４及び膜厚５０ｎｍ程度のシリコン窒化膜１０５の積層構造を形成する。これらのダミー絶縁膜及びダミーゲートは、通常の技術（酸化やＣＶＤ等の成膜技術、リソグラフィー技術、ＲＩＥ技術等）を用いて形成する。続いて、ダミーゲート（ポリシリコン膜１０４及びシリコン窒化膜１０５）をマスクとして、イオン注入技術により、ソース・ドレイン拡散層１０６となるエクステンション用の不純物拡散層を形成する。続いて、シリコン窒化膜１０７からなる幅２０～４０ｎｍ程度のゲート側壁絶縁膜を、ＣＶＤ技術とＲＩＥ技術によって形成する・（図１（ａ））。

・【００４６】次に、ダミーゲート（ポリシリコン膜１０４及びシリコン窒化膜１０５）及びゲート側壁絶縁膜・（シリコン窒化１０７）をマスクとして、イオン注入技術により、ソース・ドレイン拡散層１０８となる高濃度不純物拡散層を形成する。さらに、サリサイドプロセス技術により、ダミーゲートをマスクとしてソース・ドレイン領域のみに厚さ４０ｎｍ程度のシリサイド膜（コバルト或いはチタン等のシリサイド）１０９を形成する・（図１（ｂ））。

・【００４７】次に、層間絶縁膜１１０として、例えばシリコン酸化膜をＣＶＤ法により堆積する。さらに、この層間絶縁膜１１０をＣＭＰ技術によって平坦化することにより、シリコン窒化膜１０５及び１０７の表面を露出させる（図１（ｃ））。

・【００４８】次に、例えば燐酸を用いて、ダミーゲート上部のシリコン窒化膜１０５を層間絶縁膜１１０に対して選択的に除去する。このときに、シリコン窒化膜１０７もポリシリコン膜１０４の高さ程度までエッチングされる。続いて、例えばフッ素などのハロゲン原子のラジカルを用いたエッチング技術により、ポリシリコン膜１０４を層間絶縁膜１１０及びシリコン窒化膜１０７に対して選択的に除去する（図２（ｄ））。

・【００４９】次に、希フッ酸等のウエットエッチングによりダミーのシリコン酸化膜１０３を除去することにより、溝（凹部）１１１が形成される。続いて、ゲート絶縁膜として、高誘電体絶縁膜であるハフニウム酸化膜（HfO_2膜）を全面に形成する。このハフニウム酸化膜は、例えば、$HfCl_4$とNH_3を用いたＣＶＤ法、或いはハフニウム窒化物（ＨｆＮ）又はハフニウムのターゲットを用いたスパッタ法により、ハフニウム窒化膜・（ＨｆＮ膜）を成膜した後、成膜したハフニウム窒化膜を酸化することにより得られる（図２（ｅ））。

・【００５０】次に、ＣＶＤ法或いはスパッタ法を用いて、仕事関数が４ｅＶ程度であるハフニウム窒化膜１１３を厚さ１０ｎｍ程度、望ましくは１０ｎｍ以下で全面に成膜する（図２（ｆ））。

・【００５１】以上の図１（ａ）～図２（ｆ）の工程は、N型ＭＩＳトランジスタ形成領域及びＰ型ＭＩＳトランジスタ形成領域の双方に対して行われるが、図面上では一方の領域のみを示した。以後の工程からは、N型ＭＩＳトランジスタ（N型ＭＩＳＦＥＴ）形成領域及びＰ型ＭＩＳトランジスタ（Ｐ型ＭＩＳＦＥＴ）形成領域の双方を図面上に示す。

・【００５２】図２（ｆ）の工程の後、リソグラフィー技術を用いて、Ｐ型ＭＩＳトランジスタ形成領域以外をレジスト１１４で覆う。このときの主要部の平面図を図４・（ａ）に模式的に示す（図３（ｇ））。

・【００５３】次に、過酸化水素水によるウエットエッチングを行うことにより、Ｐ型領域のみハフニウム窒化膜１１３を除去する。このときの主要部の平面図を図４・（ｂ）に模式的に示す。ゲート絶縁膜のハフニウム酸化膜１１２は過酸化水素水に不溶であるため、エッチング

されることはない。また、ハフニウム窒化膜１１３が非常に薄い（１０ｎｍ程度）ため、従来技術の場合とは異なり、Ｎ型領域までハフニウム窒化膜１１３が深くエッチングされることはない。つまり、本例ではハフニウム窒化膜１１３の厚さが１０ｎｍ程度であるで、横方向のエッチング量Ｅも１０ｎｍ程度となる。したがって、素子間距離Ｄが２０ｎｍ程度以上であれば、従来技術の問題点を解消することができ、大幅な微細化を行うことが可能となる（図３（ｈ））。

·【００５４】次に、レジスト１１４除去した後、仕事関数が５ｅＶ程度の貴金属膜として、例えばコバルト膜１１５を全面に堆積する。コバルトの成膜は、スパッタ法を用いて行うか、或いは、Ｃｏ（ＣＯ）$_4$、Co_2（ＣＯ）$_8$、CoF_2、$CoCl_2$又は$CoBr_2$をガスソースとしたＣＶＤ法を用いて行う。その後、コバルト膜１１５、ハフニウム窒化膜１１３及びハフニウム酸化膜１１２の平坦化を、ＣＭＰ技術により、層間絶縁膜１１０が露出するまで行う。このときの主要部の平面図を図４（ｃ）に模式的に示す（図３（ｉ））。

·【００５５】以上の工程により、ゲート電極構造として、Ｎ型はハフニウム窒化膜１１３とコバルト膜１１５の積層構造からなり、Ｐ型はコバルト膜１１５の単層構造からなるＣ－ＭＩＳトランジスタが完成する。

·【００５６】本実施形態によれば、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数をＰ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数よりも小さくすることができるため（上述した例では、ハフニウム窒化膜１１３は仕事関数が４ｅＶ程度、コバルト膜１１５は仕事関数が５ｅＶ程度）、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのゲート電極の仕事関数を最適化して、両トランジスタのしきい値電圧を最適化することが可能である。

·【００５７】また、本実施形態では、Ｐ型領域のハフニウム窒化膜１１３を除去する際に、ハフニウム窒化膜１１３の膜厚が極めて薄いため、Ｎ型領域までハフニウム窒化膜１１３が深くエッチングされることを避けることができ、大幅な微細化を行うことが可能となる。さらに、本実施形態では、Ｎ型ＭＩＳトランジスタのゲート電極は、ハフニウム窒化膜１１３上に低抵抗のコバルト膜１１５が形成されているため、仕事関数の最適化と低抵抗化を両立させることができる。

·【００５８】図５は、本実施形態及び従来技術によるＮ型及びＰ型ＭＩＳトランジスタについて、しきい値（しきい電圧）の素子分離距離（素子間距離、図４に示した距離Ｄ）依存性を示したものである。

·【００５９】Ｐ型ＭＩＳトランジスタについては、本実施形態及び従来技術ともに、素子分離距離Ｄが４００ｎｍ程度まで、しきい値が一定かつ低電圧（－０．２Ｖ程度）となっている。これに対して、Ｎ型ＭＩＳトランジスタについては、従来技術では、素子間距離Ｄが３００

ｎｍ以下でしきい値が上昇し始めている。これは、Ｎ型ＭＩＳトランジスタの一部が仕事関数５．０ｅＶ程度の金属で構成されているためである。これに対して本実施形態では、素子間距離Ｄを４０ｎｍまで微細化しても、しきい値は一定であることがわかる。

·【００６０】上述した例では、Ｎ型ＭＩＳトランジスタのゲート電極がハフニウム窒化膜とコバルト膜の積層構造で、Ｐ型ＭＩＳトランジスタのゲート電極がコバルト膜の単層構造の場合について説明した。本実施形態は、このようなゲート電極構造に限らず、種々の変形が可能である。そこで、いくつかの変形例について、以下説明する。

·【００６１】本実施形態における基本的なゲート構造は、構造Ａ、構造Ｂ及び構造Ｃの３種類ある。構造Ａについては図６が、構造Ｂについては図７が、構造Ｃについては図８が、それぞれ対応している。これらの構造Ａ、構造Ｂ及び構造Ｃについては、これらの構造のバリエーションとして、例えば図９に示したような構造（構造Ｄとする）も含まれる。なお、図６～図９では、ゲート絶縁膜及びゲート電極についてのみ模式的に示している。

·【００６２】構造Ａ（図６参照）は、Ｎ型ＭＩＳトランジスタのゲート電極がゲート絶縁膜Ｆ０上に形成された第１の金属含有膜Ｆ１及び第２の金属含有膜Ｆ２からなり、Ｐ型ＭＩＳトランジスタのゲート電極がゲート絶縁膜Ｆ０上に形成された第２の金属含有膜Ｆ２からなり、第１の金属含有膜Ｆ１の仕事関数が第２の金属含有膜Ｆ２の仕事関数よりも小さい。

·【００６３】構造Ａの製造方法は、Ｎ型及びＰ型ＭＩＳトランジスタ用の双方のゲート形成領域のゲート絶縁膜Ｆ０上に第１の金属含有膜Ｆ１を形成する工程と、Ｐ型ＭＩＳトランジスタ用のゲート形成領域の第１の金属含有膜Ｆ１を除去する工程と、Ｎ型ＭＩＳトランジスタ用のゲート形成領域の第１の金属含有膜Ｆ１上及びＰ型ＭＩＳトランジスタ用のゲート形成領域のゲート絶縁膜Ｆ０上に第２の金属含有膜Ｆ２を形成することにより、Ｎ型及びＰ型ＭＩＳトランジスタの双方のゲート形成領域の凹部を埋め込む工程とからなる。

·【００６４】構造はＢ（図７参照）は、Ｐ型ＭＩＳトランジスタのゲート電極がゲート絶縁膜Ｆ０上に形成された第１の金属含有膜Ｆ１及び第２の金属含有膜Ｆ２からなり、Ｎ型ＭＩＳトランジスタのゲート電極がゲート絶縁膜Ｆ０上に形成された第２の金属含有膜Ｆ２からなり、第１の金属含有膜Ｆ１の仕事関数が第２の金属含有膜Ｆ２の仕事関数よりも小さい。

·【００６５】構造Ｂの製造方法は、Ｎ型及びＰ型ＭＩＳトランジスタ用の双方のゲート形成領域のゲート絶縁膜Ｆ０上に第１の金属含有膜Ｆ１を形成する工程と、Ｎ型ＭＩＳトランジスタ用のゲート形成領域の第１の金属含有膜Ｆ１を除去する工程と、Ｐ型ＭＩＳトランジスタ用

のゲート形成領域の第１の金属含有膜Ｆ１上及びＮ型ＭＩＳトランジスタ用のゲート形成領域のゲート絶縁膜Ｆ０上に第２の金属含有膜Ｆ２を形成することにより、Ｎ型及びＰ型ＭＩＳトランジスタの双方のゲート形成領域の凹部を埋め込む工程とからなる。

【００６６】構造Ａの具体的な例については、図１～図３で示した通りである。また、構造Ｂについては、図１～図３に示した製造方法の大部分を流用することができる（各構成材料には構造Ｂに適したものを用いる）。主要な変更点は、図３（ｇ）の工程において、Ｎ型ＭＩＳトランジスタ領域の代わりにＰ型ＭＩＳトランジスタ領域をレジストでマスクする点である。

【００６７】構造Ｃ（図８参照）は、Ｎ型ＭＩＳトランジスタのゲート電極がゲート絶縁膜Ｆ０上に形成された第１の金属含有膜Ｆ１及び第２の金属含有膜Ｆ２からなり、Ｐ型ＭＩＳトランジスタのゲート電極がゲート絶縁膜Ｆ０上に形成された第３の金属含有膜Ｆ３及び第２の金属含有膜Ｆ２からなり、第１の金属含有膜Ｆ１の仕事関数が第３の金属含有膜Ｆ３の仕事関数よりも小さい。

【００６８】構造Ｃの製造方法は（図１０参照）、Ｎ型及びＰ型ＭＩＳトランジスタ用の双方のゲート形成領域のゲート絶縁膜Ｆ０上に第１の金属含有膜Ｆ１を形成する工程と、Ｐ型ＭＩＳトランジスタ用のゲート形成領域の第１の金属含有膜Ｆ１を除去する工程と、Ｎ型ＭＩＳトランジスタ用のゲート形成領域の第１の金属含有膜Ｆ１上及びＰ型ＭＩＳトランジスタ用のゲート形成領域のゲート絶縁膜Ｆ０上に第３の金属含有膜Ｆ３を形成する工程と、Ｎ型ＭＩＳトランジスタ用のゲート形成領域の第３の金属含有膜Ｆ３を除去する工程と、Ｎ型ＭＩＳトランジスタ用のゲート形成領域の第１の金属含有膜Ｆ１上及びＰ型ＭＩＳトランジスタ用のゲート形成領域の第３の金属含有膜Ｆ３上に第２の金属含有膜Ｆ２を形成することにより、Ｎ型及びＰ型ＭＩＳトランジスタの双方のゲート形成領域の凹部を埋め込む工程とからなる。

【００６９】なお、構造Ａ、構造Ｂ及び構造Ｃには、第２の金属含有膜Ｆ２が２種類以上の積層膜である構造（構造Ｄ）も含まれる。図９の例では、図６の例に対応して、Ｎ型及びＰ型ＭＩＳトランジスタの第２の金属含有膜Ｆ２が、金属含有膜Ｆ２ａ及びＦ２ｂの積層膜によって構成されている。

【００７０】以下、上述した構造Ａ～構造Ｄについて、さらに説明する。

【００７１】（１）構造Ａ（図６参照）において、第１の金属含有膜Ｆ１は、Ｎ型ＭＩＳトランジスタのしきい値を決めるバリアメタルとして、第２の金属含有膜Ｆ２は、Ｐ型ＭＩＳトランジスタのしきい値を決めるバリアメタルとして、それぞれ用いられる。

【００７２】第１の金属含有膜Ｆ１には、Ｎ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（４．６ｅＶ以下、望ましくは４ｅＶ程度）を有し、かつダメージのないエッチング（ウエットエッチング或いはラジカル原子やラジカル分子によるドライエッチング）を行うことが可能なものを用いるようにする。代表的な材料には、ＨｆＮ及びＺｒＮがあげられる。これらは、仕事関数が４ｅＶ程度であると予想され、Ｎ型のバリアメタルとして適している。

【００７３】第２の金属含有膜Ｆ２には、Ｐ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（４．６ｅＶ以上、望ましくは５ｅＶ程度）を有し、かつゲート電極を低抵抗化できる抵抗率の低いものを用いる。貴金属系の材料は、仕事関数が５ｅＶ程度のものが多く、第２の金属含有膜に適している。抵抗率の観点からは、Ｃｏが約５$\mu\Omega$・ｃｍ、Ｎｉが約６$\mu\Omega$・ｃｍ、Ｐｔが約１０$\mu\Omega$・ｃｍである。現在ゲート電極として用いられているＷ、$CoSi_2$の抵抗率は、それぞれ約５$\mu\Omega$・ｃｍ、約２０$\mu\Omega$・ｃｍであり、Ｃｏ、Ｎｉ及びＰｔ、特にＣｏは第２の金属含有膜の材料として適している。

【００７４】ゲート絶縁膜Ｆ０については、特に限定されないが、バリアメタルがＨｆＮである場合には、HfO_2を用いることが望ましい。ＨｆＮとHfO_2との界面では熱反応が起こり難いからである。

【００７５】（２）構造Ｂ（図７参照）において、第１の金属含有膜Ｆ１は、Ｐ型ＭＩＳトランジスタのしきい値を決めるバリアメタルとして、第２の金属含有膜Ｆ２は、Ｎ型ＭＩＳトランジスタのしきい値を決めるバリアメタルとして、それぞれ用いられる。

【００７６】第１の金属含有膜Ｆ１には、Ｐ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（４．６ｅＶ以上、望ましくは５ｅＶ程度）を有し、かつダメージのないエッチング（ウエットエッチング或いはラジカル原子やラジカル分子によるドライエッチング）を行うことが可能なものを用いるようにする。代表的な材料には、WN_x及びWSi_xN_yがあげられる。

【００７７】第２の金属含有膜Ｆ２には、Ｎ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（４．６ｅＶ以下、望ましくは４ｅＶ程度）を有し、かつゲート電極を低抵抗化できる抵抗率の低いものを用いる。代表的な材料としては、Ａｌ（或いはＡｌを含む合金）があげられる。

【００７８】（３）構造Ｃ（図８参照）において、第１の金属含有膜Ｆ１はＮ型ＭＩＳトランジスタのしきい値を決めるバリアメタルとして、第３の金属含有膜Ｆ３はＰ型ＭＩＳトランジスタのしきい値を決めるバリアメタルとしてそれぞれ用いられ、第２の金属含有膜Ｆ２は低抵抗の電極材料として用いられる。

【００７９】第１の金属含有膜Ｆ１には、Ｎ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（４．６ｅＶ以下、望ましくは４ｅＶ程度）を有し、かつダメージのないエッチング（ウエットエッチング或いはラジカル原子やラジカル分子によるドライエッチング）を行う

ことが可能なもの、代表的にはＨｆＮを用いる。第３の金属含有膜Ｆ３には、Ｐ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（４．６ｅＶ以上、望ましくは５ｅＶ程度）を有し、かつダメージのないエッチングを行うことが可能なもの、代表的にはWN_xを用いる。第２の金属含有膜Ｆ２には、低抵抗である材料、代表的にはＡｌ（或いはＡｌを含む合金）を用いる。

・【００８０】（４）構造Ｄ（図９参照）における構造Ａ或いは構造Ｂに対応した構造では、積層膜である第２の金属含有膜Ｆ２として、下層側の膜Ｆ２ａについてはＮ型又はＰ型ＭＩＳトランジスタのしきい値を最適化できる仕事関数（Ｎ型については４．６ｅＶ以下、望ましくは４ｅＶ、Ｐ型については４．６ｅＶ以上、望ましくは５ｅＶ）を有していることが、上層側の膜Ｆ２ｂには低抵抗であることが求められる。

・【００８１】構造Ｄにおける構造Ｃに対応した構造では、第１の金属含有膜Ｆ１及び第３の金属含有膜Ｆ３が第２の金属含有膜Ｆ２の下にあるため、第２の金属含有膜の下層側の膜をトランジスタのしきい値を最適化するために用いるというメリットはないが、上層側からのゲート絶縁膜への金属の拡散を抑制することができるというメリットがある。

・【００８２】代表的には、構造Ａに対応した構造Ｄおいて、第１の金属含有膜Ｆ１をＨｆＮ、第２の金属含有膜の下層側Ｆ２ａをRuO_2；第２の金属含有膜の上層側Ｆ２ｂをＡｌで構成したものがあげられる。

・【００８３】（５）構造Ａ、構造Ｂ及び構造Ｃおいて、第１の金属含有膜Ｆ１には、導電体である金属化合物を用いることが望ましい。Ｎ型ＭＩＳトランジスタ用のバリアメタルとしては、ハフニウム窒化物、ジルコニウム窒化物、チタン窒化物、タンタル窒化物、タンタル窒化物、ニオブ窒化物があげられる。Ｐ型ＭＩＳトランジスタ用のバリアメタルとしては、タングステン窒化物、タングステン珪化窒化物があげられる。

・【００８４】（６）構造Ａ及び構造Ｃにおいて、第２の金属含有膜Ｆ２には、プラチナ、パラジウム、ニッケル、コバルト、ロジウム、ルテニウム、レニウム、イリジウム、金、銀、銅、或いはこれらの金属を含む合金を含む膜を用いることが望ましい。

・【００８５】（７）構造Ａ、構造Ｂ及び構造Ｃにおいて、第２の金属含有膜Ｆ２には、導電体である金属化合物を含む膜を用いることが望ましい。

・【００８６】金属化合物としては、第１に、金属酸化物・(ルテニウム酸化物、イリジウム酸化物、レニウム酸化物、プラチナ酸化物、ロジウム酸化物）があげられる。貴金属系酸化物は導電体であることが多く、Ｐ型ＭＩＳトランジスタに適した仕事関数を得やすいためである。

・【００８７】金属化合物としては、第２に、金属珪化物・(プラチナ珪化物、パラジウム珪化物、ニッケル珪化物）があげられる。これらは、Ｎ型或いはＰ型ＭＩＳトランジスタ（特にＰ型ＭＩＳトランジスタ）に適した仕事関数を得ることが可能である。

・【００８８】金属化合物としては、第３に、金属窒素化合物（ハフニウム窒化物、ジルコニウム窒化物、チタン窒化物、タンタル窒化物、ニオブ窒化物）があげられる。これらは、Ｎ型ＭＩＳトランジスタに適した仕事関数を得ることが可能である。

・【００８９】（８）構造Ｄにおいて、第２の金属含有膜Ｆ２の少なくとも最下層の膜が金属化合物であることが望ましい。金属化合物としては、金属酸化物（ルテニウム酸化物、イリジウム酸化物、レニウム酸化物、プラチナ酸化物、ロジウム酸化物）、金属珪化物（プラチナ珪化物、パラジウム珪化物、ニッケル珪化物）、金属窒素化合物（ハフニウム窒化物、ジルコニウム窒化物、チタシ窒化物、タンタル窒化物、ニオブ窒化物、タングステシ窒化物、タングステン窒化物）、タングステン窒化珪化物があげられる。

・【００９０】（９）構造Ｃにおいて、第３の金属含有膜Ｆ３には、タングステン窒化物或いはタングステン窒化珪化物を用いることが望ましい。

・【００９１】（１０）構造Ａ～構造Ｄにおいて、ゲート絶縁膜Ｆ０としては、HfO_2、ZrO_2、TiO_2、シリコン窒化膜、Al_2O_3、Ta_2O_5、Nb_2O_5、Y_2O_3、CeO_2；イットリウムを含むジルコニウム酸化膜、バリウムとストロンチウムとチタンと酸素の化合物膜、鉛とジルコニウムとチタンと酸素の化合物膜、シリコン酸化膜があげられる。

・【００９２】HfO_2、ZrO_2、TiO_2、Ta_2O_5、Nb_2O_5、Y_2O_3、CeO_2；イットリウムを含むジルコニウム酸化膜の成膜法には、それぞれ$HfCl_4$、$ZrCl_4$、$TiCl_4$、$TaCl_5$、$NbCl_5$、Ｙ（Ｔｈｄ）$_3$・(ここで、Ｔｈｄとは、２，２，６，６－テトラメチル－３，５－ヘプタネジオネートを意味する。）、Ｃｅ（Ｔｈｄ）$_4$、Ｚｒ（Ｔｈｄ）$_4$とＹ（Ｔｈｄ）$_3$の混合ガスに、O_2ガスを混入したＣＶＤ法により直接成膜する方法がある。

・【００９３】また、O_2ガスの代わりに例えばNH_3等を用いて、先ずそれぞれの金属窒化物、すなわちＨｆＮ、ＺｒＮ、ＴｉＮ、ＴａＮ、ＮｂＮ、ＹＮ、ＣｅＮ、イットリウムを含むジルコニウム窒化膜を成膜し、その後に熱酸化によってそれぞれの金属窒化物を酸化物にするようにしてもよい。この熱酸化方法を用いる場合には、窒素が膜中に残留しないように、５ｎｍ以下の窒化物を熱酸化するか、５ｎｍ以下の窒化物堆積／酸化を複数回繰り返すようにすることが望ましい。厚い窒化膜を熱酸化すると、酸化温度が５００℃以下の低温の場合に、新たに酸化された層からの生成物である窒素が膜の内部から外部に脱出できなくなり、膜中に残留してしまうことが見出されたためである。

・【００９４】また、上述した金属酸化物を成膜する前

に、熱酸化によるシリコン酸化膜、ＮＯガス中での酸化等を用いた酸化窒化膜、或いはＣＶＤ法等によるシリコシ窒化膜をシリコン基板上に成膜し、その後に上述した金属酸化膜の成膜を行うことにより、積層構造のゲート絶縁膜Ｆ０を作製してもよい。

·【００９５】（１１）ゲート電極の最下層側の膜として、ＨｆＮ、ＺｒＮ、ＴｉＮを用いる場合、これらのエッチングには過酸化水素水を用いることができる。この過酸化水素水を用いたエッチング時に、ゲート絶縁膜Ｆ０がエッチングされないことが必要である。ゲート絶縁膜Ｆ０として、上述したHfO_2、ZrO_2、TiO_2、Si_3N_4、Al_2O_3、Ta_2O_5、Nb_2O_5、Y_2O_3、CeO_2；イットリウムを含むジルコニウム酸化膜、バリウムとストロンチウムとチタンと酸素の化合物膜、鉛とジルコニウムとチタンと酸素の化合物膜、シリコン酸化膜を用いる場合には、これらは過酸化水素水に不溶であるため、問題は生じない。

·【００９６】ゲート電極の最下層側の膜として、ＴａＮ、ＮｂＮを用いる場合、これらは塩酸と硝酸の混合液に可溶である。したがって、ゲート絶縁膜Ｆ０には、この混合液に不溶であるHfO_2、ZrO_2、TiO_2、Si_3N_4；シリコン酸化膜、窒素を１％以上含有するシリコンオキシナイトライド等を用いればよい。

·【００９７】ゲート電極の最下層側の膜としてアルミニウムを用いる場合、アルミニウムは燐酸と硝酸の混合液に可溶である。したがって、ゲート絶縁膜Ｆ０には、この混合液に不溶なHfO_2、ZrO_2、TiO_2、Ta_2O_5、Nb_2O_5；イットリウムを含むジルコニウム酸化膜、バリウムとストロンチウムとチタンと酸素の化合物膜、鉛とジルコニウムとチタンと酸素の化合物膜、シリコン酸化膜を用いればよい。

·【００９８】（１２）ゲート電極の最下層側の膜として上述した金属窒化物（ＨｆＮ、ＺｒＮ、ＴｉＮ、ＴａＮ、ＮｂＮ）を用いた場合、金属窒化物膜とゲート絶縁膜との組み合わせ方は、上述したエッチング耐性の他に、次の条件を満たすことが望ましい。すなわち、金属窒化物を構成する金属元素からなる金属酸化物のＧｉｂｂｓの自由エネルギーが、ゲート絶縁膜に用いる金属酸化膜或いはシリコン酸化膜のＧｉｂｂｓの自由エネルギー以下となるようにする。このようにすると、金属窒化物がゲート絶縁膜を還元する可能性が少なくなるためである。具体的には、ゲート絶縁膜がHfO_2の場合には金属窒化物としてＨｆＮ、ＺｒＮ、ＴｉＮ、ＴａＮ、ＮｂＮを用いることが望ましく、ゲート絶縁膜がTa_2O_5の場合には金属窒化物としてＴａＮ、ＮｂＮを用いることが望ましい。

·【００９９】（実施形態２）以下、本発明の第２の実施形態に係る製造工程の一例について、図１１（ａ）～図１４（ｌ）を参照して説明する。

·【０１００】まず、シリコン基板２０１の表面を熱酸化

してシリコン酸化膜２０２を形成する。その後、ＣＶＤ法を用いて、シリコン酸化膜２０２上にシリコン窒化膜２０３を形成する（図１１（ａ））。

·【０１０１】次に、シリコン窒化膜２０３上にフォトレジスト２０４のパターンを形成する。続いて、このレジストパターン２０４をマスクにして、シリコン窒化膜２０３、シリコン酸化膜２０２及びシリコン基板２０１を異方性エッチングを用いてパターニングすることにより、素子分離溝を形成する（図１１（ｂ））。

·【０１０２】次に、フォトレジスト２０４を灰化して除去する。その後、露出している素子分離溝の表面を、例えば９５０℃、HCl/O_2雰囲気中で熱酸化することにより、シリコン酸化膜２０５を形成する。続いて、ＣＶＤ法を用いてシリコン酸化膜２０６を全面に堆積し、素子分離溝を埋め込む。さらに、ＣＭＰ法を用いてシリコン酸化膜２０６をシリコン窒化膜２０３の表面が露出するまで研磨する（図１１（ｃ））。

·【０１０３】次に、熱燐酸を用いてシリコン窒化膜２０３を選択的に除去する。続いて、希フッ酸溶液を用いてシリコン酸化膜２０２を除去する。この際に、素子分離溝の上部のシリコン酸化膜２０６及びシリコン酸化膜２０５が多少エッチングされ、素子分離溝の上部エッジ近傍のシリコン基板２０１の表面が露出する（図１２（ｄ））。

·【０１０４】次に、例えば９００℃、HCl/O_2雰囲気中で熱酸化を行い、ダミー絶縁膜となるシリコン酸化膜２０７を形成する。ダミー絶縁膜２０７は、ＭＩＳトランジスタ形成領域上だけでなく、素子分離溝の上部エッジ上にも形成されるため、シリコン基板の露出面はなくなる（図１２（ｅ））。

·【０１０５】次に、全面にポリシリコン膜２０８を形成した後、このポリシリコン膜２０８をパターニングすることにより、ダミーゲートを形成する（図１２（ｆ））。

·【０１０６】次に、ポリシリコン膜２０８からなるダミーゲートをマスクにして、シリコン基板２０１の表面に不純物イオンを注入する。さらに、高温のアニール処理を行なうことにより、ソース・ドレイン拡散層２０９をダミーゲートに対して自己整合的に形成する。続いて、全面に層間絶縁膜２１０を堆積し、この層間絶縁膜２１０をＣＭＰ法を用いてポリシリコン膜２０８が露出するまで平坦化する。その後、露出したポリシリコン膜２０８を、例えばCF_4/O_2ガスを用いたダウンフロー技術で除去する（図１３（ｇ））。

·【０１０７】次に、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのしきい値電圧の調整を行なうために、露出したダミー絶縁膜２０７を介して、シリコン基板２０１中にそれぞれＮ型及びＰ型の不純物をイオン注入法で導入する。続いて、ダミー絶縁膜２０７を希フッ酸溶液を用いて除去することにより、溝（凹部）２１１が形成され

る。その後、ゲート絶縁膜として、Ta_2O_5膜２１２を形成する。さらに、Ｐ型ＭＩＳトランジスタのゲート電極材料として、ルテニウム（Ｒｕ）膜又はパラジウム（Ｐｄ）膜２１３を、膜厚１０ｎｍ程度形成する（図１３（ｈ））。

【０１０８】次に、プラズマＣＶＤ法により、全面にシリコン窒化膜２１４を１０ｎｍの膜厚で形成する。このシリコン窒化膜２１４は、後の工程で形成されるインジウム（Ｉｎ）又はスズ（Ｓｎ）の拡散を防止するための拡散防止膜として用いられる。その後、Ｐ型ＭＩＳトランジスタ領域上にフォトレジスト２１５のパターンを形成する（図１３（ｉ））。

【０１０９】次に、露出したＮ型ＭＩＳトランジスタ領域のシリコン窒化膜２１４を、ダウンフロー法を使って除去する。フォトレジスト２１５を灰化処理によって除去した後、Ｎ型ＭＩＳトランジスタのゲート電極材料として、全面にインジウム（Ｉｎ）膜又はスズ（Ｓｎ）膜を１～２ｎｍの膜厚で形成する（図１４（ｊ））。

【０１１０】次に、２００℃～４００℃程度の中低温アニールを行う。Ｐ型ＭＩＳトランジスタ領域にはシリコン窒化膜２１４が形成されているため、このアニール処理により、Ｎ型ＭＩＳトランジスタ領域にのみ選択的にインジウム又はスズが拡散する。インジウム又はスズは、ルテニウム膜又はパラジウム膜２１３の結晶粒界を通って拡散する。これにより、インジウム又はスズが、ゲート絶縁膜となるTa_2O_5膜２１２とルテニウム膜又はパラジウム膜２１３との界面に析出する。その結果、Ｎ型ＭＩＳトランジスタのゲート電極となるインジウム膜又はスズ膜２１６が形成される（図１４（ｋ））。

【０１１１】次に、Ｐ型ＭＩＳトランジスタ領域上のインジウム膜又はスズ膜２１６を選択的に除去し、さらにシリコン窒化膜２１４をダウンフロー法を使って除去する。その後、タングステン膜２１７をＮ型及びＰ型ＭＩＳトランジスタのゲート電極領域の溝に埋め込む。さらに、ＣＭＰ法を用いて、溝外のルテニウム膜又はパラジウム膜２１３、インジウム膜又はスズ膜２１６、Ta_2O_5膜２１２及びタングステン膜２１７を除去し、溝内にのみタングステン膜２１７を残す。これにより、Ｐ型ＭＩＳトランジスタではルテニウム膜又はパラジウム膜２１３が最下層に形成されたゲート電極が、Ｎ型ＭＩＳトランジスタではインジウム膜又はスズ膜２１６が最下層に形成されたゲート電極が構成される。以降、層間絶縁膜２１８、配線２１９等を形成し、半導体集積回路が完成する（図１４（ｌ））。

【０１１２】なお、上述した例では、Ｐ型ＭＩＳトランジスタのゲート電極を構成する金属Ｍ１（上述した例では、ルテニウム又はパラジウム）中をＮ型ＭＩＳトランジスタのゲート電極を構成する金属Ｍ２（上述した例では、インジウム又はスズ）を拡散させることにより、金

属Ｍ２をＮ型ＭＩＳトランジスタのゲート絶縁膜界面に析出させるようにしたが、金属Ｍ２を金属Ｍ１中に拡散させることにより金属Ｍ１と金属Ｍ２との合金を形成し、この合金によってＮ型ＭＩＳトランジスタのゲート電極を構成するようにしてもよい（変形例１とする）。

【０１１３】また、上述した例では、Ｐ型ＭＩＳトランジスタのゲート電極を構成する金属Ｍ１中をＮ型ＭＩＳトランジスタのゲート電極を構成する金属Ｍ２を拡散させる際に、シリコン窒化膜２１４を拡散のマスクとして用いることにより、金属Ｍ２を選択的にＮ型ＭＩＳトランジスタ領域に拡散させるようにしたが、シリコン窒化膜２１４は形成せずに、Ｎ型ＭＩＳトランジスタ領域の金属Ｍ１上にのみ金属Ｍ２を選択的に形成し、上述した例と同様に、Ｎ型ＭＩＳトランジスタ領域でのみ選択的に金属Ｍ２を金属Ｍ１中に拡散させるようにしてもよい（変形例２とする）。

【０１１４】さらに、上述した基本例及び変形例１、２は、金属Ｍ２をゲート絶縁膜界面に析出させる、或いは金属Ｍ１と金属Ｍ２との合金を形成するという方法を、Ｎ型ＭＩＳトランジスタのゲート電極に対して行っているが、同様の方法をＰ型ＭＩＳトランジスタのゲート電極に対して行ってもよい。

【０１１５】本実施形態によれば、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数をＰ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数よりも小さくすることができるため、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのゲート電極の仕事関数を最適化して、両トランジスタのしきい値電圧を最適化することが可能である。また、本実施形態では、ゲート電極形成用の溝内に形成された金属膜を従来のようにエッチング除去しないため、ゲート絶縁膜の信頼性の低下を抑制することが可能である。

【０１１６】（実施形態３）以下、本発明の第３の実施形態に係る第１の例について、その製造工程の一例を図１５（ａ）～図１７（ｈ）を参照して説明する。

【０１１７】まず、シリコン基板３０１上に素子分離３０２を形成し、続いて、Ｎ型ＭＩＳトランジスタ領域にＰ型のウエル拡散層３０３を、Ｐ型ＭＩＳトランジスタ領域にＮ型のウエル拡散層３０４を形成する（図１５（ａ））

次に、露出しているシリコン基板３０１の表面を５ｎｍ程度酸化して、ダミー絶縁膜となるシリコン酸化膜３０５を形成する。その後、ダミーゲートとなるポリシリコン膜３０６を堆積し、これをゲート電極の形状にパターニングする。続いて、ダミーゲートとなるポリシリコ膜３０６をマスクにして、Ｎ型領域に砒素を、Ｐ型領域に硼素をイオン注入し、ソース・ドレイン拡散層３０７となる浅い不純物拡散層を形成する。その後、シリコン窒化膜３０８を堆積し、これを異方性エッチングすることにより、側壁絶縁膜を形成する。続いて、この側壁絶縁

膜３０８及びポリシリコン膜３０６をマスクにして、Ｎ型領域に砒素を、Ｐ型領域に硼素をイオン注入し、ソース・ドレイン拡散層３０９となる深い不純物拡散層を形成する（図１５（ｂ））。

【０１１８】次に、全面に層間絶縁膜３１０としてシリコン酸化膜を堆積する。その後、ＣＭＰ法を用いて、シリコン酸化膜３１０をポリシリコン膜３０６が露出するまで平坦化する（図１５（ｃ））。

【０１１９】次に、ケミカルドライエッチング等の等方性エッチング技術を用いて、ポリシリコン膜３０６を除去する。続いて、露出したシリコン酸化膜３０５を希フッ酸処理等によりエッチング除去し、Ｎ型及びＰ型ＭＩＳトランジスタ領域の双方にゲート電極形成用の溝３１１を形成する（図１６（ｄ））。

【０１２０】次に、熱酸化処理によってゲート電極形成用の溝３１１底部のシリコン基板３０１を酸化し、シリコン酸化膜３１２からなるゲート絶縁膜を形成する。続いて、Ｎ型ＭＩＳトランジスタのゲート電極材料として、ＣＶＤ法によりタングステンシリサイド（WSi_2）膜３１３を全面に堆積する。その後、ＣＭＰ法によりゲート電極形成用の溝３１１の外部に堆積されたタングステンシリサイド膜３１３を除去し、ゲート電極形成用の溝３１１内にのみタングステンシリサイド膜３１３を残置させる（図１６（ｅ））。

【０１２１】次に、全面にシリコン窒化膜３１４を堆積し、さらにフォトリソグラフィー及びエッチング技術によって、Ｎ型ＭＩＳトランジスタ領域にのみシリコン窒化膜１５を残置させる。続いて、スパッタ法等により、パラジウム（Ｐｄ）膜３１５を全面に堆積する（図１６（ｆ））。

【０１２２】次に、６００℃、１分間程度のアニール処理を行う。これにより、Ｐ型ＭＩＳトランジスタ領域のゲート電極部分に埋め込まれているタングステンシリサイド膜３１３がパラジウム膜３１５と反応する。その結果、もともとタングステンシリサイド膜３１３の存在した領域にパラジウムシリサイド（Pd_2Si）膜３１６が形成され、このパラジウムシリサイド膜３１６の上部のパラジウム膜中にタングステンが排出される。Ｎ型ＭＩＳトランジスタ領域では、シリコン窒化膜３１４形成されているため、タングステンシリサイド膜３１３はパラジウムシリサイド膜３１６に置換されない。その後、ＣＭＰ等により、ゲート電極形成用の溝の外部に残った金属及びシリコン窒化膜３１４を除去する。これにより、Ｐ型ＭＩＳトランジスタのゲート電極がパラジウムシリサイド膜３１６によって形成される（図１７（ｇ））。

【０１２３】次に、全面に層間絶縁膜３１７となるシリコン酸化膜を堆積する。続いて、ＭＩＳトランジスタのソース・ドレイン及びゲート電極に達するコンタクト用の穴を、層間絶縁膜３１７及び３１０に形成する。その

後、配線３１８用の金属膜を堆積して、これをパターニングすることにより、Ｎ型及びＰ型のＭＩＳトランジスタトランジスタが完成する（図１７（ｈ））。

【０１２４】なお、上述した例では、Ｎ型ＭＩＳトランジスタのゲート電極材料としてタングステンシリサイド（WSi_2）膜を用いたが、タングステンシリサイドの代わりに、モリブデンシリサイド（$MoSi_2$）、タンタルシリサイド（$TaSi_2$）、ニオブシリサイド（$NbSi_2$）或いはクロムシリサイド（$CrSi_2$）等のシリサイドを用いることも可能である。

【０１２５】また、上述した例では、Ｐ型ＭＩＳトランジスタ領域のタングステンシリサイド膜上にパラジウム（Ｐｄ）膜を形成し、熱処理によってパラジウムをタングステンシリサイド膜と反応させることにより、タングステンシリサイドをパラジウムシリサイド（Pd_2Si、ＰｄＳｉ）に置換するようにしたが、パラジウムの代わりにニッケル（Ｎｉ）或いはプラチナ（Ｐｔ）を用い、ニッケルシリサイド（ＮｉＳｉ、$NiSi_2$）或いはプラチナシリサイド（Pt_2Si、ＰｔＳｉ）等のシリサイドに置換することも可能である。

【０１２６】また、上述した例（以下の第２及び第３の例でも同様）では、ゲート絶縁膜として熱処理によって得られたシリコン酸化膜を用いるようにしたが、ＣＶＤ法等によって形成したTa_2O_5膜を用いるようにしてもよい。

【０１２７】次に、本発明の第３の実施形態に係る第２の例について、その製造工程の一例を図１８（ａ）～図１８（ｃ）を参照して説明する。

【０１２８】なお、途中の工程（図１５（ａ）～図１６（ｅ）の工程）までは上述した第１の例と同様であるため、本例では図１６（ｅ）の工程よりも後の工程について説明する。

【０１２９】図１６（ｅ）の工程の後、レジスト３２１でＮ型ＭＩＳトランジスタ領域をマスクした後、イオン注入法によって、Ｐ型ＭＩＳトランジスタ領域のタングステンシリサイド膜３１３にのみ選択的にゲルマニウムイオン（Ge^+）をイオン注入し、ゲルマニウムを含むタングステンシリサイド膜３１３ａとする。このとき、タングステンシリサイド膜３１３に導入するゲルマニウムイオンの濃度は、タングステンシリサイド中におけるゲルマニウムの固溶限以上の濃度、例えば$1\times10^{17}cm^{-3}$程度とする（図１８（ａ））。

【０１３０】次に、レジスト３２２でＰ型ＭＩＳトランジスタ領域をマスクし、イオン注入法によって、Ｎ型ＭＩＳトランジスタ領域のタングステンシリサイド膜３１３にのみ選択的にインジウムイオン（In^+）をイオン注入し、インジウムを含むタングステンシリサイド膜３１３ｂとする。このとき、タングステンシリサイド膜３１３に導入するインジウムイオンの濃度は、タングステンシリサイド中におけるインジウムの固溶限以上の濃

度、例えば$1\times10^{17}cm^{-3}$程度とする（図１８（ｂ））。

【０１３１】次に、８００℃、１分程度の熱処理を行うことにより、タングステンシリサイド膜３１３中に注入されたゲルマニウム及びインジウムが、タングステンシリサイド膜３１３とゲート絶縁膜であるシリコン酸化膜３１２との界面に析出する。その結果、Ｐ型ＭＩＳトランジスタではゲルマニウム膜３２３及びタングステンシリサイド膜３１３の積層構造によってゲート電極が形成され、Ｎ型ＭＩＳトランジスタではインジウム膜３２４及びタングステンシリサイド膜３１３の積層構造によってゲート電極が形成される（図１８（ｃ））。

【０１３２】最後に、第１の例と同様に、層間絶縁膜を堆積してコンタクト用の穴を開け、さらに配線を形成することにより、Ｎ型及びＰ型のＭＩＳトランジスタが完成する。

【０１３３】なお、上述した例では、ゲート電極用の溝の中に予め形成しておく材料としてタングステンシリサイド（WSi_2）膜を用いたが、タングステンシリサイドの代わりに、モリブデンシリサイド（$MoSi_2$）、タンタルシリサイド（$TaSi_2$）、ニオブシリサイド（$NbSi_2$）或いはクロムシリサイド（$CrSi_2$）を用いることも可能である。

【０１３４】また、上述した例では、ゲート絶縁膜界面に析出させる材料として、Ｐ型ＭＩＳトランジスタではゲルマニウム（Ｇｅ）、Ｎ型ＭＩＳトランジスタではインジウム（Ｉｎ）を用いたが、ゲルマニウム、インジウム、アンチモン（Ｓｂ）、プラチナ（Ｐｔ）、パラジウム（Ｐｄ）等の中から適当な材料を選択して、Ｐ型及びＮ型の両トランジスタで別々の材料を析出させるようにしてもよい。また、これらの材料をＰ型又はＮ型の一方のトランジスタについてのみ析出させ（一方のトランジスタについてのみイオン注入を行い）、他方のトランジスタではもともとのゲート電極材料（上述した例ではタングステンシリサイド）をそのままゲート電極として用いるようにしてもよい。

【０１３５】さらに、上述した例では、イオン注入した物質を熱処理によってゲート絶縁膜界面に析出させるようにしたが、Ｐ型及びＮ型ＭＩＳトランジスタのゲート電極領域に別々の物質をイオン注入し、熱処理等によってイオン注入した各物質とゲート電極領域にもともと形成されていたゲート電極材料との反応物を形成し、Ｎ型ＭＩＳトランジスタの反応物の仕事関数がＰ型ＭＩＳトランジスタの反応物の仕事関数よりも小さくなるようにしてもよい。

【０１３６】次に、本発明の第３の実施形態に係る第３の例について、その製造工程の一例を図１９（ａ）～図１９（ｃ）を参照して説明する。

【０１３７】なお、途中の工程（図１５（ａ）～図１６（ｄ）の工程）までは上述した第１の例と同様であるため、本例では図１６（ｄ）の工程よりも後の工程について説明する。

【０１３８】図１６（ｅ）の工程の後、ゲート電極形成用の溝に、スパッタ法とＣＭＰ法とを用いて、Ｐ型ＭＩＳトランジスタのゲート電極材料として、ニッケル（Ｎｉ）膜３３１を埋め込む（図１９（ａ））。

【０１３９】次に、全面にアモルファスシリコン（ａ－Ｓｉ）膜３３２をスパッタ法等によって堆積した後、Ｎ型ＭＩＳトランジスタ領域上以外の領域のアモルファスシリコン膜３３２をフォトリソグラフィー法とドライエッチング法等を用いて除去する（図１９（ｂ））。

【０１４０】次に、４００℃、１分程度の熱処理を加えることにより、Ｎ型ＭＩＳトランジスタ領域のゲート電極部分において、ニッケル膜３３１とアモルファスシリコン膜３３２を反応させ、ニッケルシリサイド（ＮｉＳｉ）膜３３３を形成する。その後、反応に寄与しなかったアモルファスシリコン膜３３２を、ケミカルドライエッチング等の等方性エッチングによって除去する。このようにニッケル膜３３１をニッケルシリサイド膜３３３に変化させることにより、材料の仕事関数を５．０ｅＶ程度から４．３６ｅＶ程度にまで低下させることができる（図１９（ｃ））。

【０１４１】最後に、第１の例と同様に、層間絶縁膜を堆積してコンタクト用の穴を開け、さらに配線を形成することにより、Ｎ型及びＰ型のＭＩＳトランジスタトランジスタが完成する。

【０１４２】なお、上述した例では、Ｐ型ＭＩＳトランジスタのゲート電極をニッケル（Ｎｉ）、Ｎ型ＭＩＳトランジスタのゲート電極をニッケルシリサイド（ＮｉＳｉ、$NiSi_2$）としたが、コバルト（Ｃｏ）とコバルトシリサイド（$CoSi_2$）、クロム（Ｃｒ）とクロムシリサイド（$CrSi_2$）、モリブデン（Ｍｏ）とモリブデンシリサイド（$MoSi_2$）等で形成してもよい。

【０１４３】本実施形態によれば、Ｎ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数をＰ型ＭＩＳトランジスタのゲート絶縁膜に接する部分の仕事関数よりも小さくすることができるため、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのゲート電極の仕事関数を最適化して、両トランジスタのしきい値電圧を最適化することが可能である。また、本実施形態では、ゲート電極形成用の溝内に形成された金属膜を従来のようにエッチング除去しないため、ゲート絶縁膜の信頼性の低下を抑制することが可能である。

【０１４４】以上、本発明の実施形態を説明したが、本発明は上記実施形態に限定されるものではなく、その趣旨を逸脱しない範囲内において種々変形して実施することが可能である。

【０１４５】

【発明の効果】本発明によれば、Ｎ型及びＰ型ＭＩＳトランジスタそれぞれのゲート電極の仕事関数を最適化す

ることにより、Ｎ型及びＰ型ＭＩＳトランジスタのしきい値電圧を最適化することが可能である。また、半導体装置の微細化、低抵抗化を達成することが可能であり、さらにゲート電極等の信頼性を向上させることが可能となる。

・【図面の簡単な説明】

・【図１】本発明の第１の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図２】本発明の第１の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図３】本発明の第１の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図４】本発明の第１の実施形態に係る半導体装置の製造方法によって得られる効果について示した平面図。

・【図５】本発明の第１の実施形態に係る半導体装置の製造方法によって得られるＭＩＳトランジスタについて、そのしきい値の素子間距離依存性を従来技術と対比して示した図。

・【図６】本発明の第１の実施形態に係る半導体装置の基本構成の一例を模式的に示した図。

・【図７】本発明の第１の実施形態に係る半導体装置の基本構成の他の例を模式的に示した図。

・【図８】本発明の第１の実施形態に係る半導体装置の基本構成の他の例を模式的に示した図。

・【図９】本発明の第１の実施形態に係る半導体装置の基本構成の他の例を模式的に示した図。

・【図１０】図８に示した基本構成を得るための主要な製造工程について示した図。

・【図１１】本発明の第２の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図１２】本発明の第２の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図１３】本発明の第２の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図１４】本発明の第２の実施形態に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図１５】本発明の第３の実施形態に係る半導体装置の製造方法の一例について、その工程の一部を示した工程断面図。

・【図１６】本発明の第３の実施形態に係る半導体装置の製造方法の一例について、その工程の一部を示した工程断面図。

・【図１７】本発明の第３の実施形態に係る半導体装置の製造方法の一例について、その工程の一部を示した工程断面図。

・【図１８】本発明の第３の実施形態に係る半導体装置の

製造方法の他の例について、その工程の一部を示した工程断面図。

・【図１９】本発明の第３の実施形態に係る半導体装置の製造方法の他の例について、その工程の一部を示した工程断面図。

・【図２０】従来技術に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図２１】従来技術に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図２２】従来技術に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図２３】従来技術に係る半導体装置の製造方法について、その工程の一部を示した工程断面図。

・【図２４】従来技術に係る半導体装置の製造方法の問題点について示した平面図。

・【符号の説明】

１０１…シリコン基板
１０２…素子分離
１０３…シリコン酸化膜
１０４…ポリシリコン膜
１０５、１０７…シリコン窒化膜
１０６、１０８…ソース・ドレイン拡散層
１０９…シリサイド膜
１１０…層間絶縁膜
１１１…溝
１１２…ハフニウム酸化膜
１１３…ハフニウム窒化膜
１１４…レジスト
１１５…コバルト膜
２０１…シリコン基板
２０２、２０５、２０６、２０７…シリコン酸化膜
２０３、２１４…シリコン窒化膜
２０４、２１５…レジスト
２０８…ポリシリコン膜
２０９…ソース・ドレイン拡散層
２１０、２１８…層間絶縁膜
２１１…溝
２１２…Ta_2O_5膜
２１３…Ｒｕ膜又はＰｄ膜
２１６…Ｉｎ膜又はＳｎ膜
２１７…タングステン膜
２１９…配線
３０１…シリコン基板
３０２…素子分離
３０３…Ｐ型ウエル
３０４…Ｎ型ウエル
３０５、３１２…シリコン酸化膜
３０６…ポリシリコン膜
３０７、３０９…ソース・ドレイン拡散層
３０８、３１４…シリコン窒化膜

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３１０、３１７…層間絶縁膜
３１１…溝
３１３…タングステンシリサイド膜
３１５…パラジウム膜
３１６…パラジウムシリサイド膜
３１８…配線

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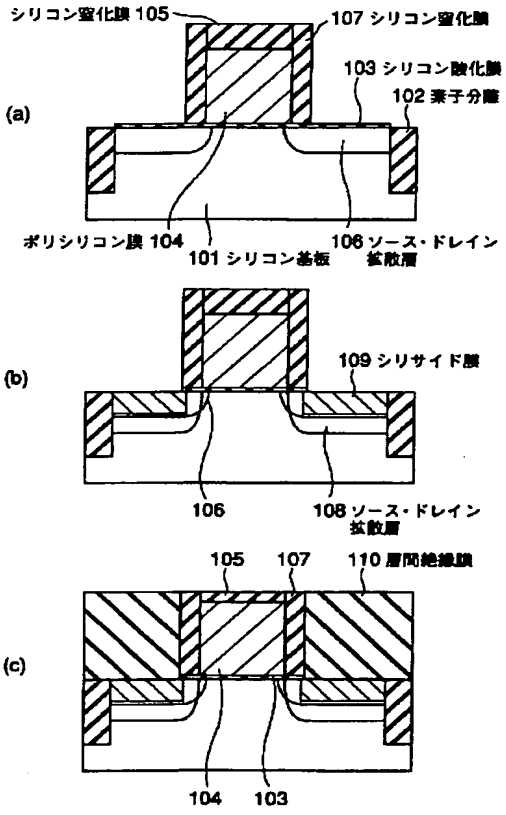
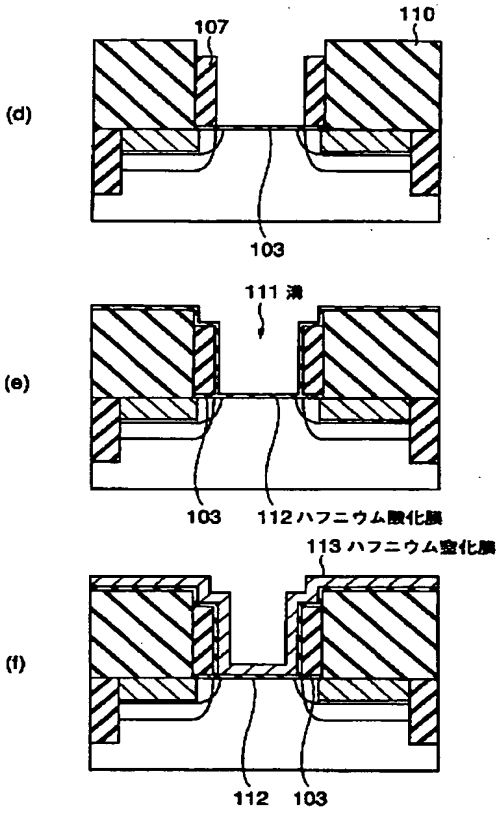
＊３２１、３２２…レジスト
３２３…ゲルマニウム膜
３２４…インジウム膜
３３１…ニッケル膜
３３２…アモルファスシリコン膜
＊　３３３…ニッケルシリサイド膜

・【図１】



・【図２】



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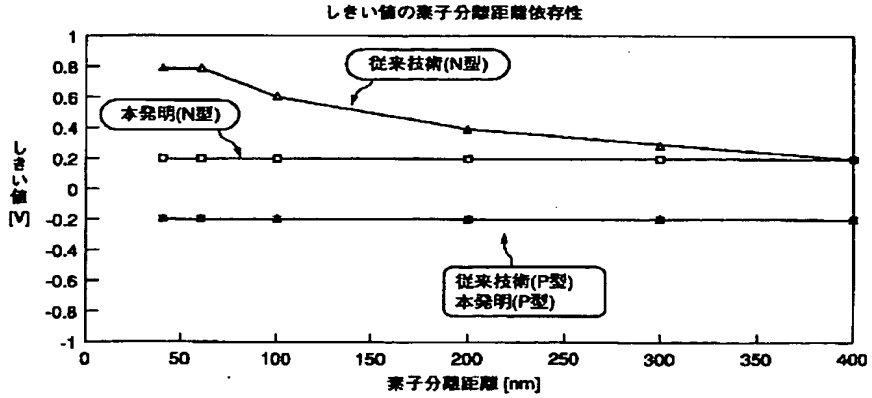

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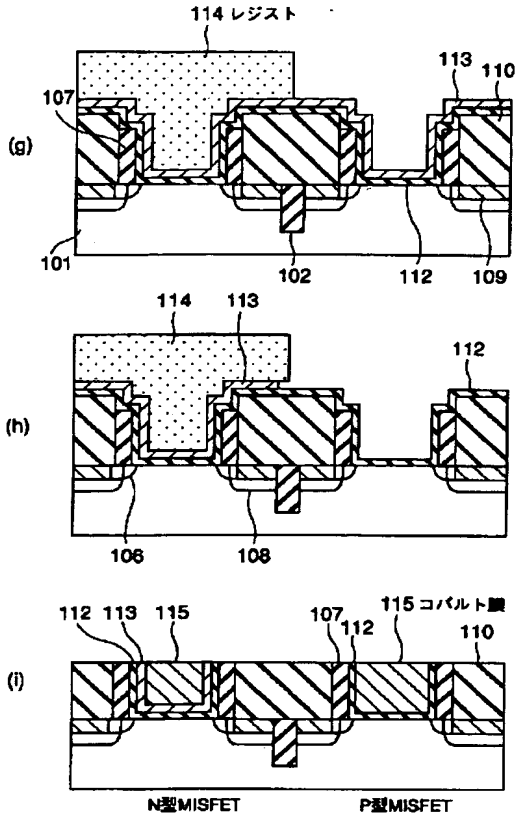

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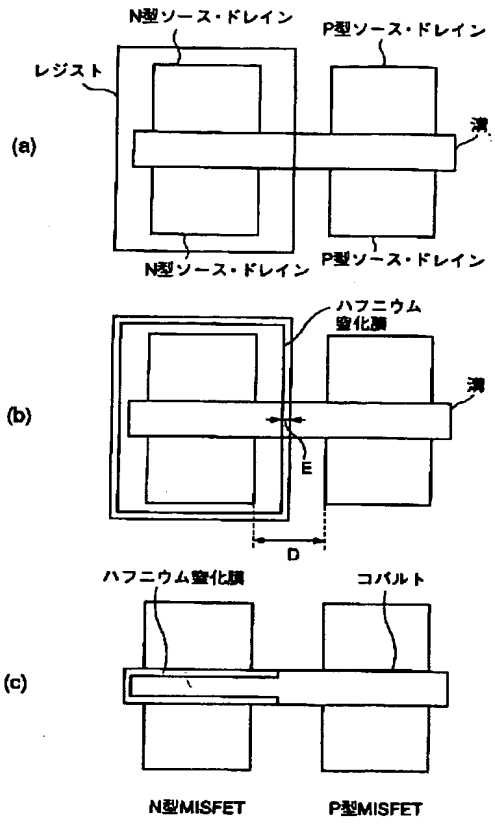

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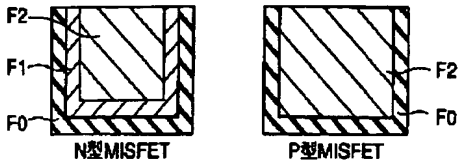

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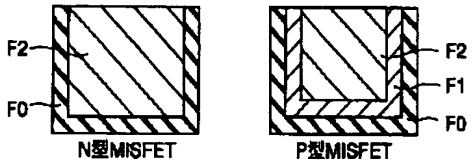

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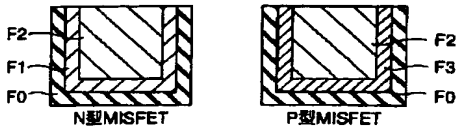

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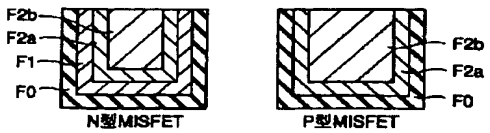
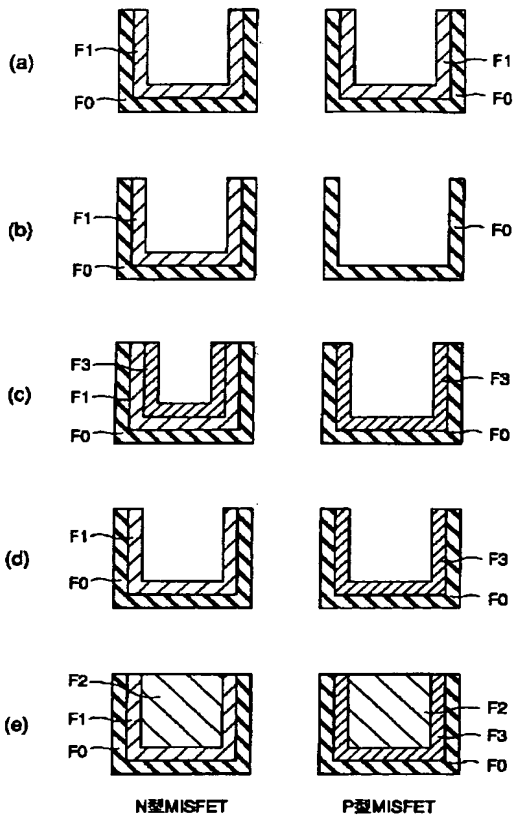
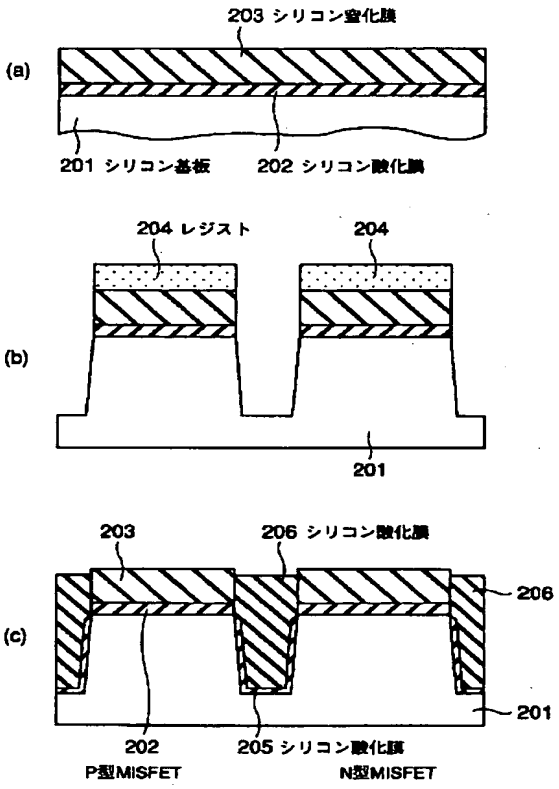


・【図１０】



・【図１１】



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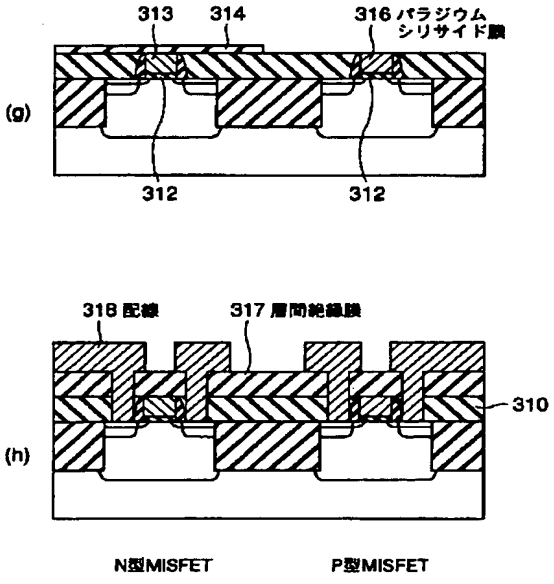

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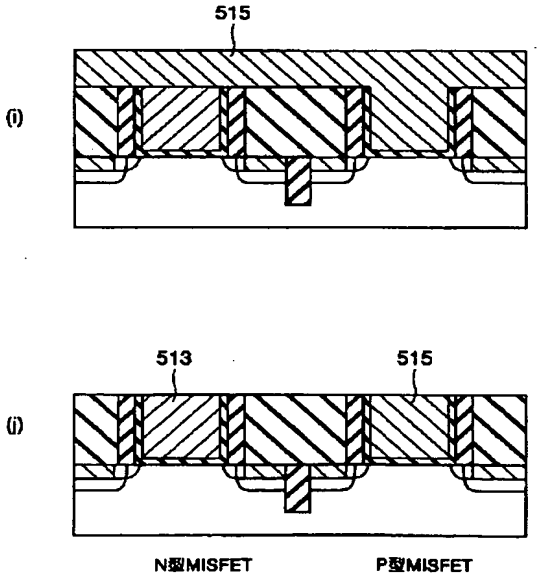
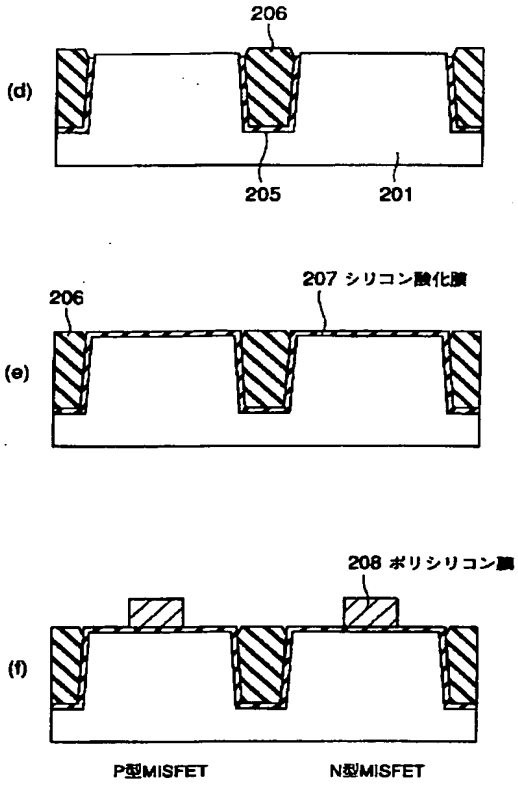
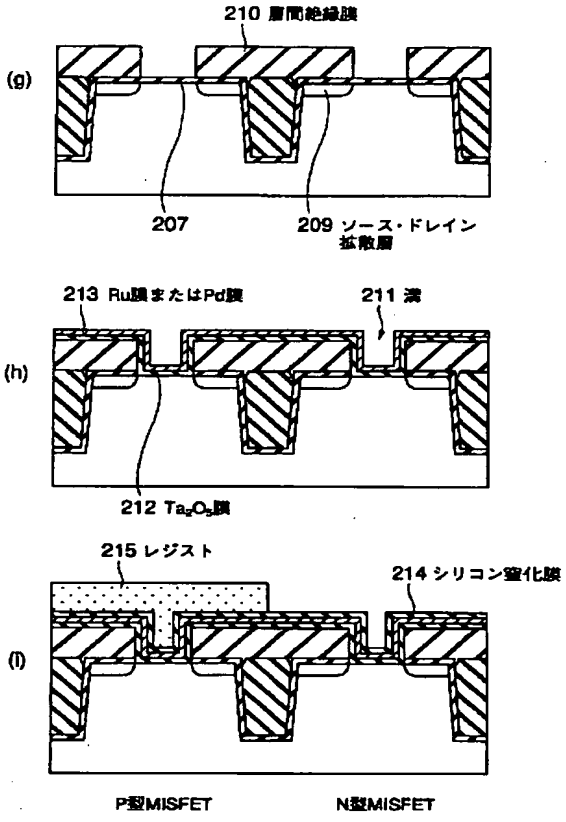


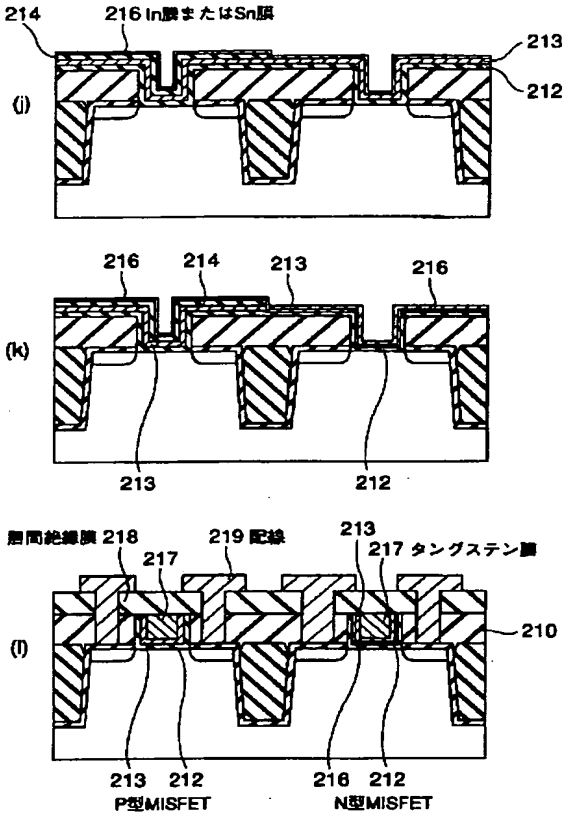
・【図１２】


(d)
206
205
201
(e)
206
207 シリコン酸化膜
(f)
208 ポリシリコン膜
P型MISFET
N型MISFET

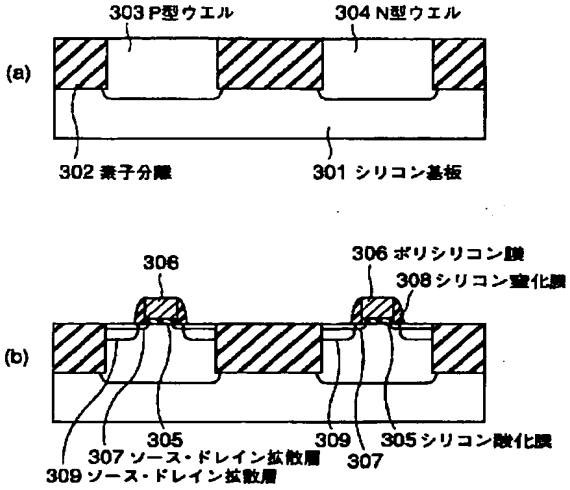
・【図１３】


(g)
210 層間絶縁膜
207
209 ソース・ドレイン
拡散層
(h)
213 Ru膜またはPd膜
211 溝
212 Ta_2O_5膜
(i)
215 レジスト
214 シリコン窒化膜
P型MISFET
N型MISFET

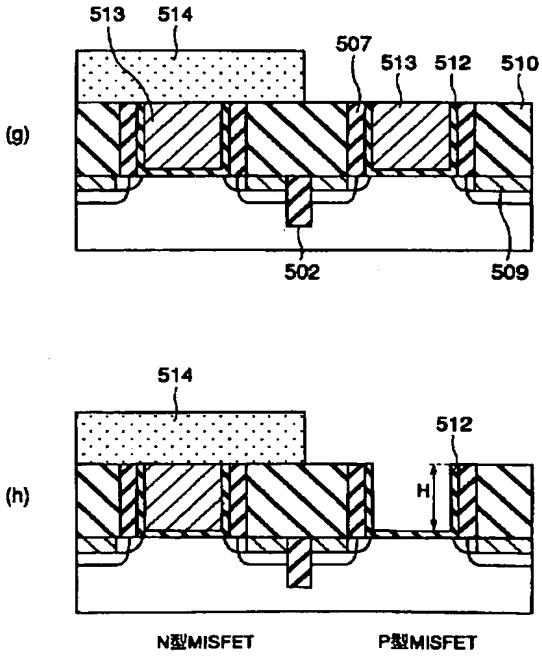
・【図１４】


214
216 In膜またはSn膜
213
212
(j)
216
214
213
216
(k)
213
212
層間絶縁膜 218
217
219 配線
213
217 タングステン膜
210
(l)
213
212
216
212
P型MISFET
N型MISFET

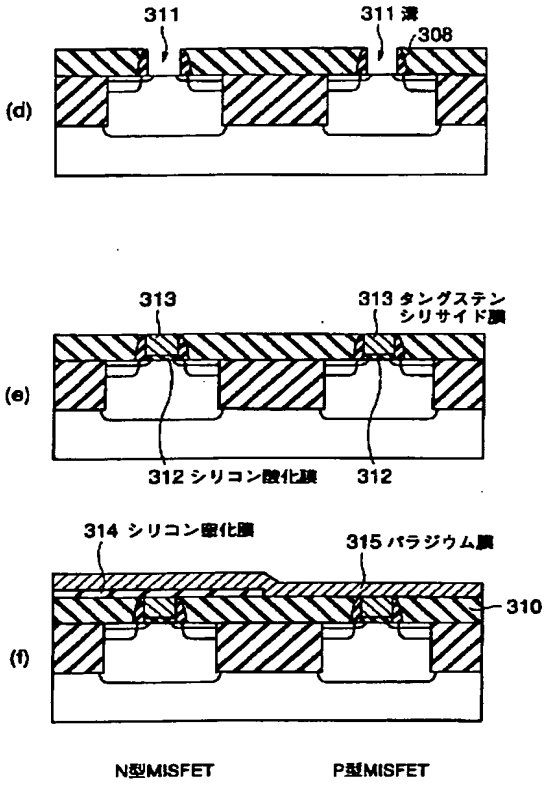
・【図１５】


303 P型ウエル
304 N型ウエル
(a)
302 素子分離
301 シリコン基板
306
306 ポリシリコン膜
308 シリコン窒化膜
(b)
305
309
305 シリコン酸化膜
307 ソース・ドレイン拡散層
307
309 ソース・ドレイン拡散層
310 層間絶縁膜
(c)
305
N型MISFET
P型MISFET

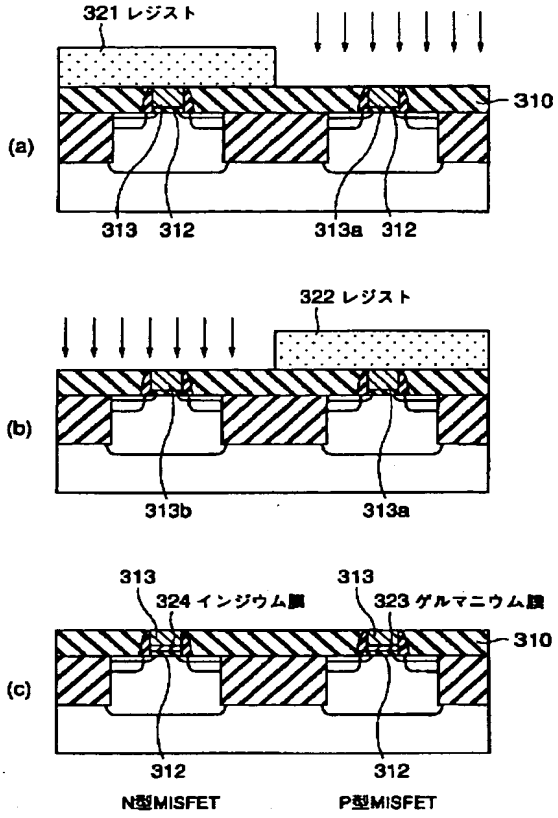
・【図２２】


513
514
507
513
512
510
(g)
502
509
514
512
H
(h)
N型MISFET
P型MISFET

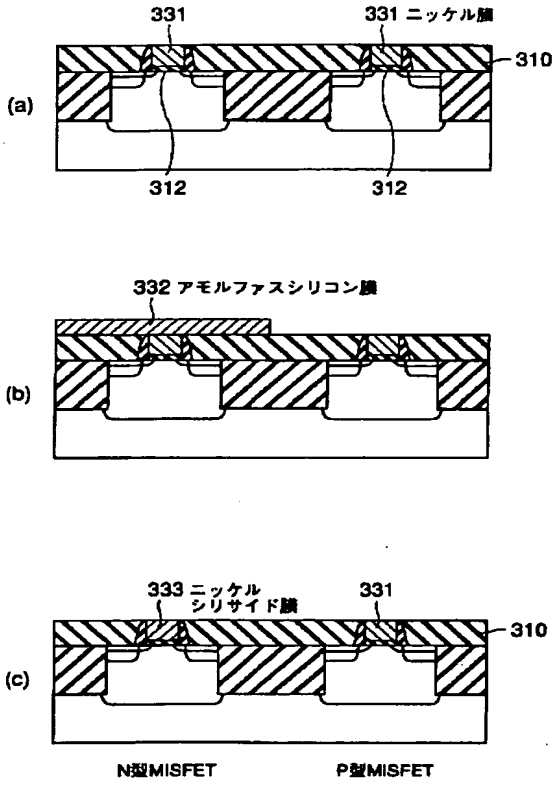
・【図１６】


311
311 溝
308
(d)
313
313 タングステン
シリサイド膜
(e)
312 シリコン酸化膜
312
314 シリコン窒化膜
315 パラジウム膜
310
(f)
N型MISFET
P型MISFET

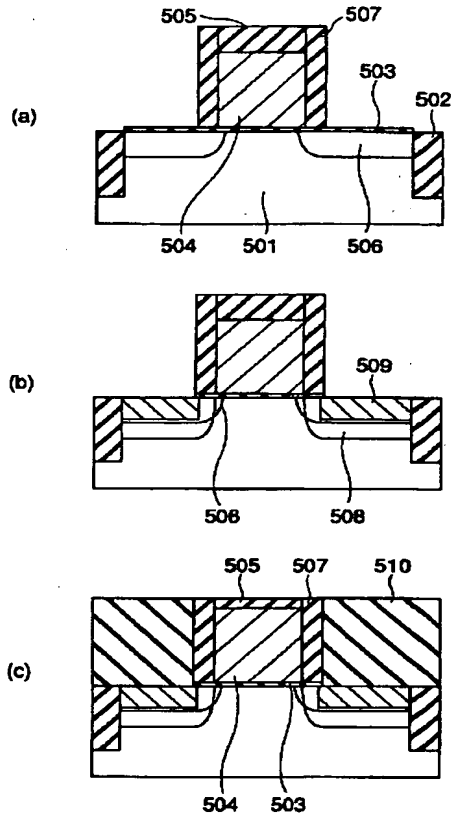
・【図１８】


321 レジスト
310
(a)
313
312
313a
312
322 レジスト
(b)
313b
313a
313
313
324 インジウム膜
323 ゲルマニウム膜
310
(c)
312
312
N型MISFET
P型MISFET

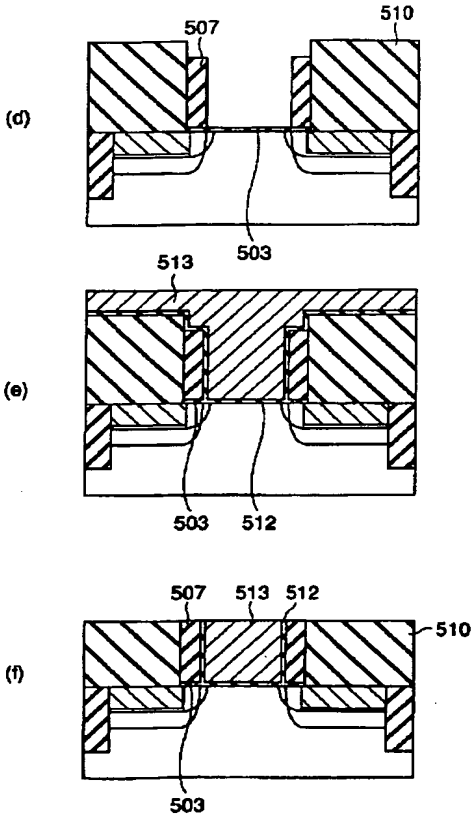
・【図１９】


(a)
331
331 ニッケル膜
310
312
312
(b)
332 アモルファスシリコン膜
(c)
333 ニッケル
シリサイド膜
331
310
N型MISFET
P型MISFET

・【図２０】


(a)
505
507
503
502
504
501
506
(b)
509
508
508
(c)
505
507
510
504
503

【図２１】



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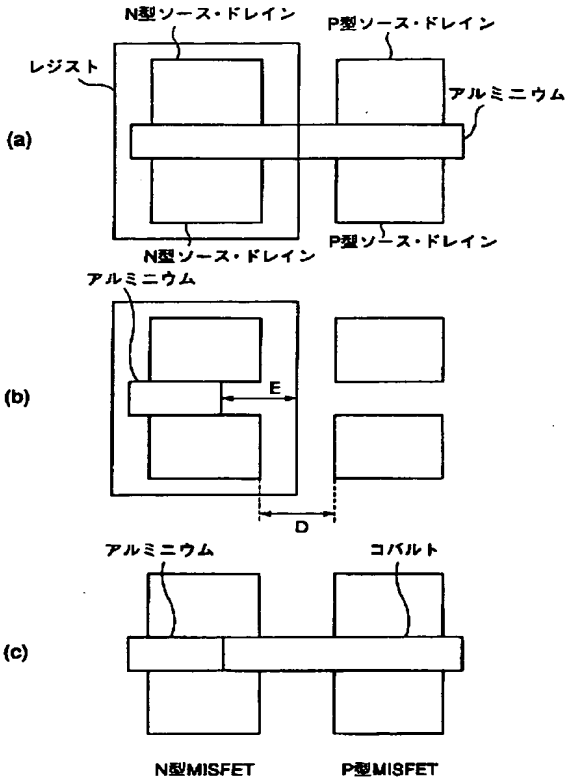

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